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Josephson Waveforms Characterization of a Sigma-Delta Analog-to-Digital Converter for Data Acquisition in Metrology

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Josephson Waveforms Characterization of a Sigma-Delta Analog-to-Digital Converter for Data Acquisition in Metrology

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To my fiancée Teresa,
to my mother and
to the memory of Norma Rodríguez

Abstract

A sampling system based on a 24-bits sigma-delta analog-to-digital converter (ADC) was built and characterized in order to study the feasibility of using this type of ADCs in electrical metrology.

The non-linearities of the sampling system have been studied and a model for post-correcting the measured data points established. The Hammerstein model, consisting of a static non-linear part and a linear system, was employed. A 4-th order polynomial accounts for the non-linearities of the analog electronics and the input stages of the sigma delta ADC. The linear part corresponds to the transfer function of the decimation filters internal to the ADC. The parameters for the model of the system were determined using noiseless and drift-free waveforms from a Josephson waveform synthesizer.

The performance of the sampling system was verified experimentally by comparing the measured root-mean-square (rms) value of sinusoidal signals with the results from an established method. The results obtained using the post-corrected samples from the sampling system at 125 Hz agreed to within 2 μV/V with the *de facto* standard in metrology laboratories, which uses a high accuracy digital voltmeter.

Precision measurements are limited by the decimation filters inside the ADC and can only be carried out for frequencies below 1/24-th of the equivalent sampling rate. The characterization results have shown that the non-linearities have been compensated to 5 μV/V or better and the effective resolution exceeds 20 bits, over an input range of 1 V at the equivalent sampling rate of 32 kHz. The experimental validation has proved that it is possible to measure rms values of sinusoidal signals with 1 V peak amplitudes for frequencies up to 1.3 kHz with uncertainty of 8 μV/V, significantly improving the uncertainty achievable with *de facto* standard which reaches 8 μV/V at 500 Hz.

Kurzfassung

Ein Abtastsystem basierend auf einem 24-Bit Sigma-Delta Analog-Digital Wandler (ADC) wurde gebaut und charakterisiert, um die Möglichkeiten eines solchen ADC-Typs für Anwendungen in der elektrischen Metrologie zu untersuchen.

Die Nichtlinearitäten des Abtastsystems wurden bestimmt und ein Modell für die nachträgliche Korrektur der erfassten Abtastwerte entwickelt. Dafür wurde das Hammerstein Modell verwendet, das zur Charakterisierung eines statisch, nichtlinearen Blocks gefolgt von einem linearen Teil geeignet ist. Ein Polynom vierter Ordnung wurde zur Beschreibung der statischen Nichtlinearität in der analogen Elektronik und der Eingangsstufe des Sigma-Delta ADC verwendet. Der lineare Teil des Modells umfasst die Transferfunktion des Dezimationsfilters im ADC Chip. Die Parameter für das Modell wurden mithilfe rausch- und driftloser Signale von einem Josephson Wellenform Synthesizer ermittelt.

Die Leistungsfähigkeit des Abtastsystems wurde experimentell durch Effektivwertmessungen (rms) von sinusförmigen Signalen mit einem etablierten Messverfahren überprüft. Als Ergebnis wurde eine Übereinstimmung innerhalb von 2 μV/V bei 125 Hz mit dem *de facto* Normal der metrologischen Kalibrierlabore gefunden, das auf einem hochpräzisen Digitalvoltmeter basiert.

Präzisionsmessungen haben ergeben, dass die Dezimationsfilter im ADC die maximale Frequenz auf 1/24stel der äquivalenten Abtastrate begrenzen, wenn die bestmöglichen Unsicherheiten erreicht werden sollen. Die Ergebnisse der Systemcharakterisierung haben bestätigt, dass Nichtlinearitäten auf 5 μV/V oder besser kompensiert werden. Die effektive Auflösung überschreitet 20 Bit über einen Eingangsbereich von 1 V und mit einer äquivalenten Abtastrate von 32 kHz. Die experimentelle Überprüfung hat gezeigt, dass es mit dem neuen System möglich ist, den Effektivwert sinusförmiger Signale und 1 V Amplitude für Frequenzen bis 1,3 kHz mit einer Messunsicherheit von 8 μV/V zu bestimmen, und somit die erreichbare Messunsicherheit des *de facto* Normals, das 8 μV/V bei 500 Hz erreicht, deutlich zu verbessern.

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Chapter 1

Introduction

Most national metrology institutes (NMIs) have employed sampling techniques for ac metrology applications during the last two decades. Mainly, this technique is based on using an integrating analogue-to-digital converter (IADC) as sampler. A high accuracy digital voltmeter, the Agilent 3458A, is widely used at most NMIs as sampler and its performance for metrology applications has been checked and published [1, 2]. The aim of this thesis is to study the feasibility of using sigma-delta analog-to-digital converters for ac metrology applications. To accomplish this objective, a sampling system to measure rms values of ac quantities in the frequency range from 60 Hz to 2 kHz to achieve a combined uncertainty in the order of 5 μV/V was designed, modeled and characterized using Josephson waveforms [3].

Sigma-Delta analog-to-digital converters (Σ-Δ ADC) have recently become more attractive for high precision sampling applications due to their improved low-noise characteristics, high resolution and low non-linearity [4]. An initial evaluation of such a device, carried out at PTB, confirmed their feasibility for high-grade metrology applications [5]. As a result, a sampling system built around such a Σ-Δ ADC has been designed, incorporating the expertise gained in such research.

Studies have been conducted to characterize the dynamic and static metrological behavior of ADCs. Hence, standards of The Institute of Electrical and Electronics Engineers (IEEE), the IEEE standard 1057-1994 [6] and the IEEE standard 1241-2001 [7], report methods to carry out performance tests. In this work, because of the low uncertainty requirement in the calibration, the characterization of the Σ-Δ ADC was performed by means of the Josephson Waveform Synthesizer. This quantum standard is a powerful tool because of its intrinsic characteristics of noiseless, non-drift and its inherent accuracy that are exploited in methods described herein. Moreover, it assures traceability to the SI unit of voltage [8], which can be reproduced with an accuracy of a few parts in 10^{10} [9].

Metrology applications demand high accuracy in the determination of the measurand. A practical ADC cannot provide the needed performance due to imperfections such as gain deviation, thermal drift, non-linearity and others. As a consequence, the ADC readouts will have deviations from the original signal applied to its input. With an ADC characterization these deviations can be quantified and, in most cases, corrected and/or post-compensated by modeling the ADC in order to reconstruct the input signal with high accuracy. For many years, researches have been interested in ADC modeling, therefore, several models, such as based on power series expansion, lock up table, model inversion and block-oriented models, have been studied [10, 11]. As Σ-Δ ADCs are difficult to describe mathematically, researches used behavioral models to simulate and post-compensate the deviations of ADCs [12]. The internal structure of a Σ-Δ ADC includes an analog part, which consists of a modulator or a cascade of modulators (in a multistage topology) and a digital part with a quantizer and several digital decimation filters [4]. The analog part may have non-linear behavior due to imperfections and mismatch in the components, being its most critical part the front-end modulator [13, 14]. The digital part commonly includes a cascade of linear finite impulse response filters. Therefore, the internal architecture of a Σ-Δ ADC is a cascade of a non-linear system with a linear system. A model that offers non-linear and linear representation is a block oriented model, the Hammerstein model [15] which is made up of a cascade of two blocks, a non-linear block at the input stage connected to a linear block. In this thesis, the parameters of this model were found to post-compensate the ADC readouts in order to reconstruct the original input signal. For the non-linear block a polynomial representation has been chosen, while the linear block models the frequency response of the decimation filters of the Σ-Δ ADC.

The model should be experimentally validated in order to assess whether the parameters of the model are suitable or not to reach the targeted performance. For such purpose, the performance of the Σ-Δ sampling system has been evaluated under sinusoidal excitation in the frequency range from 62.5 Hz to 2 kHz at maximum amplitude equal to 1 V.

Furthermore, ADC performance metrics such as total harmonic distortion, interharmonic product distortion, signal-to-noise ratio are important to determine. The dynamic behavior of the ADC can be described using them although, as will become clear, their relevance for metrology applications is limited. These metrics can be characterized by means of the Josephson Arbitrary Waveform Synthesizer which generates spectrally pure sinusoidal signal and multi-tone sinusoidal signals [16].

Settling time and noise are other important metrics of Σ-Δ ADCs. The decimation filters used in Σ-Δ ADCs severely restrict the settling times that can be achieved with

this architecture. The settling time adds transients which introduce errors in the results when measuring alternating signals with spectra made up of numerous frequencies, harmonically related or not.

Noise will degrade the signal-to-noise ratio and in consequence will limit the achievable effective resolution of the ADC. The Josephson Waveform Synthesizer, which can generate stepwise approximated waveforms and dc values, is the most suitable system to determine these two parameters because of its lack of drift and noise at the output.

This thesis starts with an introduction to Σ-Δ ADCs in chapter 2. Chapter 3 describes the system hardware and includes an analysis of the sources of deviations. The ADC model and parameter identification are then introduced and the uncertainty contribution evaluated. The performance dynamic metrics characterization are presented in chapter 5. Chapter 6 covers the parameter identification of the Hammerstein model and the additional compensation required to compute the rms value of the signal to be measured. Finally, chapter 7 summarizes and discusses the experimental validation of the ADC model when measuring sinusoidal signals.

Chapter 2

Introduction to Sigma-Delta Data Converters

This chapter reports a brief introduction to the analog-to-digital conversion process, analyzes the quantization noise and presents a brief description of a linear model of quantizers. Then, it follows with an introduction and theoretical background regarding sigma-delta analog-to-digital converters (ADC). It starts with a first order modulator and ends with a multistage modulator. The advantages of sigma-delta ADCs over Nyquist rate ADCs are examined. Finally, it presents the internal structure of the device used in this thesis.

2.1 Analog-to-Digital Conversion

An analog-to-digital converter (ADC) converts a continuous-time signal to a discrete-time sequence. The process involves two operations: i) to take samples of the continuous signal $x_c(t)$ at periodic intervals T_s, commonly denominated *sampling time* (the reciprocal of T_s is the *sampling frequency* f_s) to produce a discrete-time sequence $x[n]$ according to the relation [17]

$$x[n] = x_c(nT_s) \qquad -\infty < n < \infty, \tag{2.1}$$

and ii) amplitude quantization by mapping the signal $x[n]$ into digital levels $\tilde{x}[n]$ by a system called *Quantizer*. The first operation is known as *sampling* and the second operation is known as *quantization*. The analog-to-digital conversion is depicted in figure 2.1.

In a practical setting, these operations are implemented by an analog-to-digital converter (ADC).

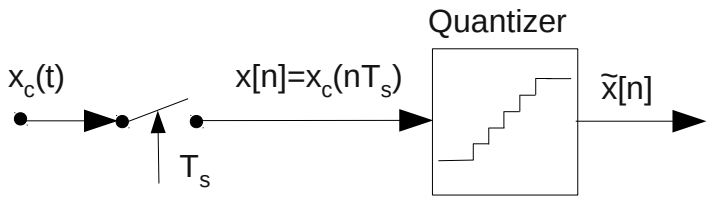

Figure 2.1: Simplified diagram of the analog-to-digital conversion process

2.1.1 The Nyquist Sampling Theorem

The conversion process of $x_c(t)$ to a sequence $x[n] = x_c(nT_s)$ represented in figure 2.1 can be mathematically stated as a modulation of the continuous-time signal $x_c(t)$ by a periodic impulse train $s(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$ with period T_s, where $\delta(t)$ is the Dirac delta function, hence

$$x[n] = x_c(nT_s)s(t) = \sum_{n=-\infty}^{\infty} x_c(nT_s)\delta(t - nT_s). \tag{2.2}$$

Applying the Fourier transform [17] to equation (2.2) follows that the Fourier transform of $x[n]$ is the convolution product of the Fourier transform $X_c(j2\pi f)$ of $x_c(nT_s)$ and the Fourier transform $S(j2\pi f)$ of the periodic impulse train $s(t)$:

$$X(j2\pi f) = \frac{1}{2\pi} X_c(j2\pi f) * S(j2\pi f) \tag{2.3}$$

Since the Fourier transform of a periodic impulse train is [17]

$$S(j2\pi f) = \frac{2\pi}{T_s} \sum_{k=-\infty}^{\infty} \delta(2\pi f - k2\pi f_s), \tag{2.4}$$

then

$$X(j2\pi f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X_c(j2\pi f - jk2\pi f_s), \tag{2.5}$$

with f_s the sampling frequency. Equation (2.5) states that the Fourier transform of the sampled signal $x[n]$ consists of periodic copies of the Fourier transform of the continuous time signal $x_c(nT_s)$ at the sampling frequency f_s as represented in figure 2.2.

If the signal to be sampled contains frequencies above f_N, i.e. if $f_N \geq f_s/2$, the copies of $X(j2\pi f)$ overlap, so that the original signal is not longer recoverable due to an effect known as *aliasing*. The aliasing effect is depicted in figure 2.3, where the signal $x_c(t)$ has frequency components that overlap when sampled at f_s.

Therefore, if the signal $x_c(t)$ is ideally band-limited to f_N it can be sampled without

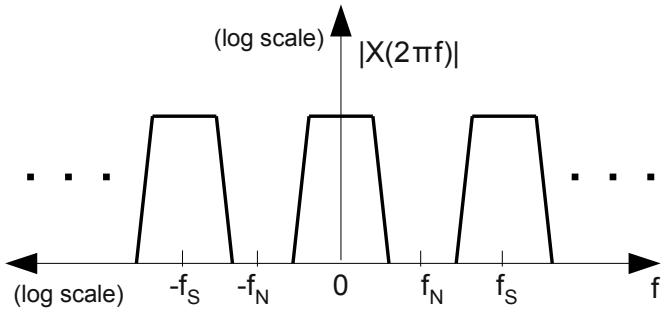

Figure 2.2: Fourier transform of an ideally band-limited signal $x[n]$ to f_N sampled at f_s

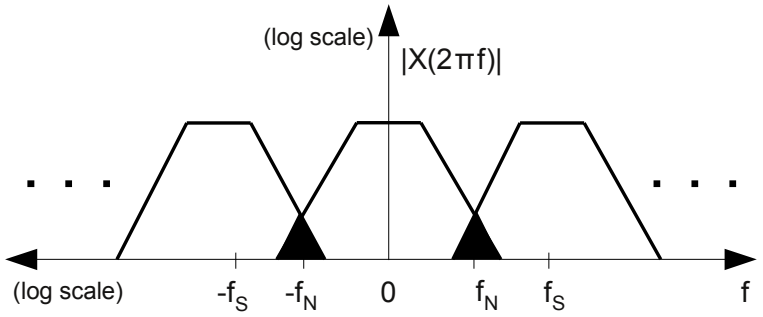

Figure 2.3: Fourier transform of $x[n]$. The new discrete-time signal has new frequency components (shadowed areas) because of aliasing.

adding or losing information. This is the basis of the **Nyquist sampling theorem**, stated as:

> *If $x_c(t)$ is a band-limited signal to f_N. Then $x_c(t)$ is uniquely represented by the sequence $x[n] = x_c(n/f_s)$, $n \in \mathbb{Z}$ if,*
>
> $$f_N < \frac{f_s}{2}. \tag{2.6}$$
>
> The frequency f_N is known as the *Nyquist frequency.*

2.2 Quantization Process

After sampling the analogue input signal it is quantized in amplitude to a defined number of output values by the quantizer, a block diagram of a quantizer is depicted in figure 2.4.

A typical characteristic of an uniform ideal quantizer is shown in figure 2.5. It illustrates some features of quantizers:

i) according to the separation of the output levels, quantizers can be classified in two groups:

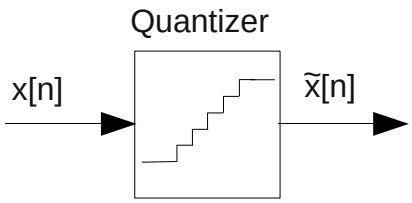

Figure 2.4: Quantizer block diagram

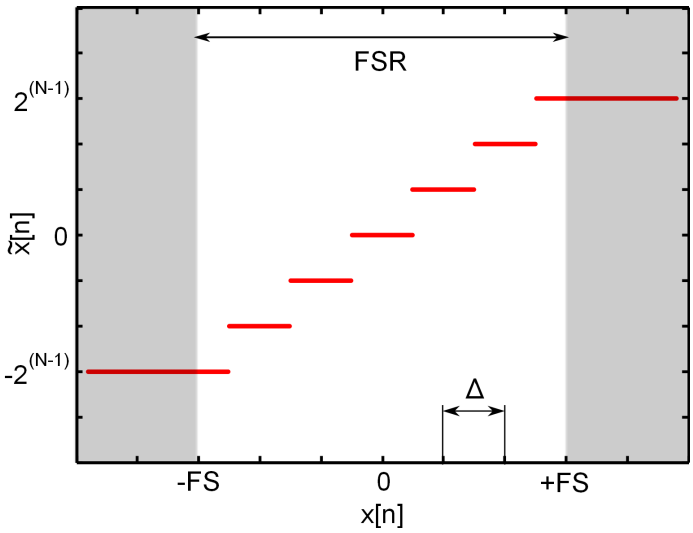

Figure 2.5: Typical characteristic of an ideal quantizer. The input signal $x[n]$ is mapped into different output levels represented by $\tilde{x}[n]$

- uniform quantizers, the quantization levels are equally spaced, or
- nonuniform quantizers,

ii) depending on the input signal span they can be:

- bipolar, if the input signal has positive and negative values or
- unipolar,

iii) a N-bit quantizer has 2^N output levels with the signal being assigned to 2^{N-1} intervals, thus the distance Δ between decision boundaries is

$$\Delta = \frac{FSR}{2^N} = \frac{2 \cdot FS}{2^N} = \frac{FS}{2^{N-1}}, \tag{2.7}$$

where FSR is the input full-scale range (FSR=$2FS$, FS full-scale),

iv) the input signal of the quantizer should be in the FSR interval, otherwise the quantizer is *overloaded* and the output is clamped to the maximum (or minimum) output level (the *overloaded* regions are illustrated as shadows in figure 2.5),

v) the difference between two adjacent output levels is one least significant bit (LSB) of 2^N output levels, where N is the resolution in bits of the quantizer,

vi) the quantizer characteristic is non-linear and non invertible, since input amplitude values that are within one input level produce the same output level,

vii) depending on the quantizer characteristic they can be classified in two types:

- *mid-tread quantizer*: if the output level $\tilde{x}[n] = 0$ occurs in the middle of the flat portion (depicted in figure 2.5).
- *mid-rise quantizer*: if the output level $\tilde{x}[n] = 0$ occurs at the edge of the level transition.

The main feature of a mid-tread quantizer is that the quantizer has a zero output level, thus there is no output offset when the input signal is zero. This characteristic is usually preferred. The main disadvantage is that to produce a symmetric transfer function the number of output levels in mid-tread quantizers has to be odd. Since an odd number is not a power of two, to accomplish a symmetrical output characteristic the number of output levels has to be increased [17, 18].

2.2.1 Quantizer Linear Model

The process of quantization is deterministic and therefore an error signal $e[n]$ is determined by the difference between the output $\tilde{x}[n]$ and the input $x[n]$ as

$$e[n] = \tilde{x}[n] - x[n]. \tag{2.8}$$

The error signal $e[n]$ is depicted in figure 2.6 for an uniform, bipolar mid-tread quantizer.

A simple model for the quantizer is depicted in figure 2.7. The output signal of the quantizer $\tilde{x}[n]$ can be written as

$$\tilde{x}[n] = x[n] + e[n]. \tag{2.9}$$

In this model the error signal $e[n]$ is considered as an additive noise signal. To apply the model some assumptions regarding the input and error signals have to be considered: i) the input signal $x[n]$ has to remain within the input range of the quantizer and to change in large amounts so that the position in quantization levels is random, ii) the error $e[n]$ is uncorrelated with the input signal.

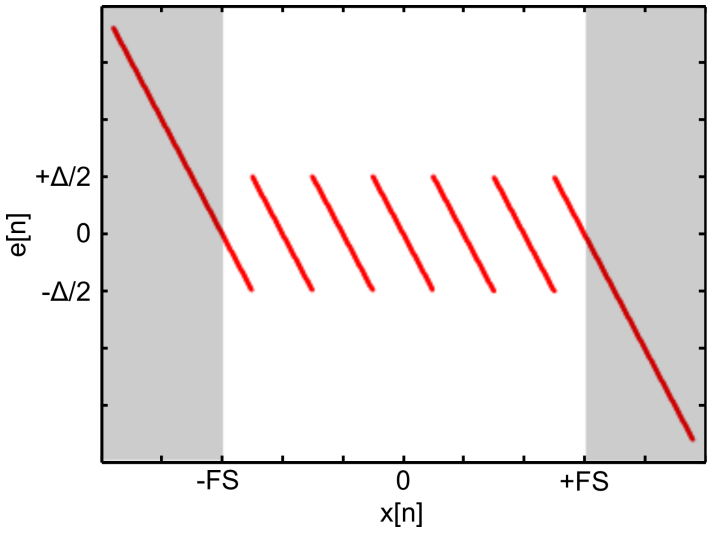

Figure 2.6: Quantization error signal for a mid-tread quantizer

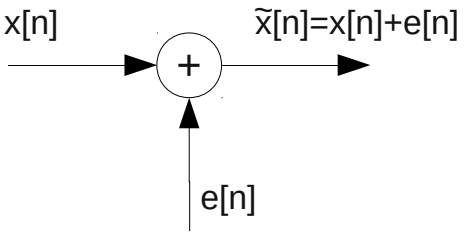

Figure 2.7: Lineal model for a quantizer

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With these assumptions the error signal $e[n]$ can be treated as a stochastic process uniformly distributed within the range $[-\Delta/2, \Delta/2]$ [17, 19, 20]; the first-order probability density function for the quantization error is shown in figure 2.8.

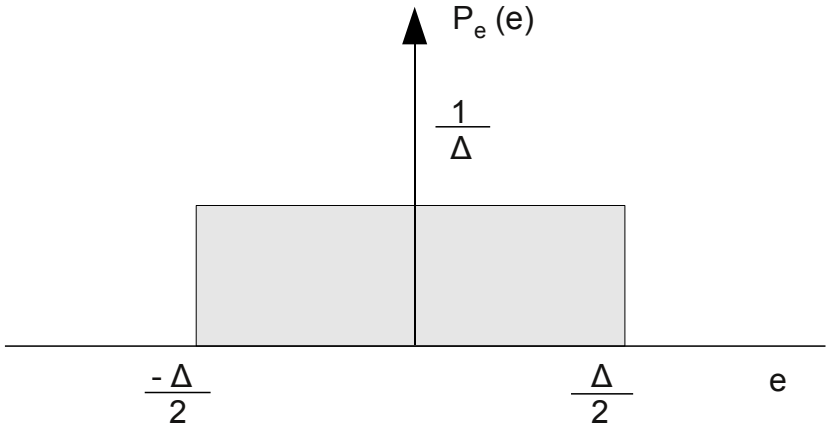


Figure 2.8: Probability density function of quantization error $e[n]$

Hence, $e[n]$ can be considered as a white noise process with zero mean and variance

equal to [17]:

$$\sigma_e{}^2 = \frac{\Delta^2}{12}, \tag{2.10}$$

$e[n]$ is commonly referred, in the literature, as *quantization noise* [17, 18].

Now it is possible to compute the degradation added by the quantization noise to the signal using the signal-to-noise ratio (SNR). If the input signal has a variance (power) equal to σ_s^2, then the signal-to-noise ratio in decibels (dB) is:

$$SNR = 10\log\left(\frac{\sigma_s^2}{\sigma_e^2}\right) = 20\log\left(\frac{\sigma_s}{\sigma_e}\right). \tag{2.11}$$

Replacing equation (2.7) and (2.10) into equation (2.11),

$$\begin{aligned} SNR &= 20\log\left(\frac{\sigma_s}{\Delta}\cdot\sqrt{12}\right) \\ &= 20\log\left(\frac{\sigma_s}{FS}\right) + 6.02N + 4.77. \end{aligned} \tag{2.12}$$

If a sinusoidal signal of amplitude equal to full scale is applied to the quantizer; its root-mean-squared (rms) value is $\frac{FS}{\sqrt{2}}$, hence $\sigma_s = \frac{FS}{\sqrt{2}}$. Replacing σ_s in equation (2.12), the signal-to-noise ratio in dB becomes:

$$SNR = 6.02N + 1.76, \tag{2.13}$$

with N the resolution in bits of the quantizer. This equation gives the theoretical SNR for a quantizer of N-bits resolution. Due to imperfections in the quantizer and its associated circuitry, the practical SNR is lower than the theoretical value. Therefore, a new metric is introduced to determine the practical resolution of the quantizer, the *effective number of bits* (ENOB), defined as:

$$ENOB = \frac{SNR - 1.76}{6.02}. \tag{2.14}$$

2.2.2 Complete Analog-to-Digital Conversion Process

The complete analog-to-digital conversion process can be summarized as follows: samples $x[n]$ of the analog input signal $x_c(t)$ are taken at equally spaced intervals T_s, then the quantizer takes these samples and produces the output $\tilde{x}[n]$. At the end, a coder translates to a binary codification, such as bipolar offset binary, binary two's complement [21], the output signal $\tilde{x}[n]$ of the quantizer to obtain a digital representation $x_B[n]$ of the analog input signal $x_c(t)$. The complete process is shown in figure 2.9.

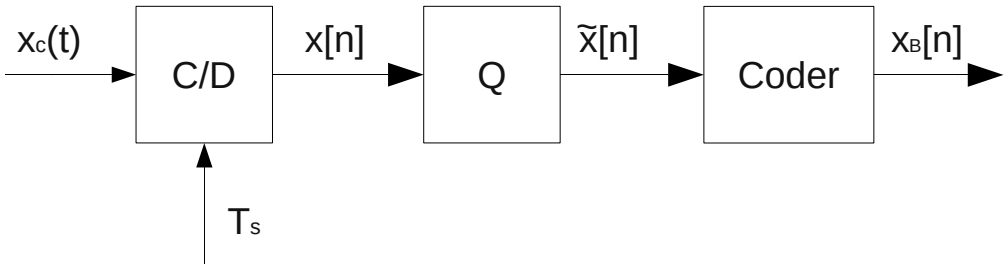


Figure 2.9: Analogue-to-digital conversion process

2.3 Sigma-Delta Analog-to-Digital Converters

Analog-to-digital converters (ADC) can be classified in two basic types:

- *Nyquist-rate* and
- *Oversampled*.

When an ADC samples a continuous-time signal at double of the highest frequency component present on the signal is the case of *Nyquist-rate* ADCs. In other words, a Nyquist-rate ADC samples a continuous-time signal band-limited to f_B at a sampling rate $f_s = 2f_B$, therefore the input signal can be reconstructed according to the Nyquist theorem (see section 2.1.1). An oversampling ADC samples the same continuous-time signal at a sampling rate $f_s \gg f_B$ [4].

Integrating, flash, pipeline and successive approximation converters belong, in general, to the Nyquist-rate category, while sigma-delta converters belong to the oversampled category.

Oversampling converters offer several advantages over Nyquist-rate converters such as relaxation on the anti-aliasing filter design, high resolution, low non-linearity and quantization noise shaping [4, 18].

A simple diagram for a sigma-delta (Σ-Δ) analog-to-digital converter is presented in figure 2.10. On it two main parts are distinguished: a) an analog part and b) a digital part. The analog part consists of a Σ-Δ modulator which samples the analog input signal at a high sampling rate, and the digital part, that consists of a digital low-pass filter (LPF) followed by a decimator or compressor [17], has the task of down-sampling the output of the modulator in order to reduce the signal bandwidth to the band of interest [4, 22].

2.3.1 Sigma-Delta Modulator

A basic scheme for a Σ-Δ modulator is shown in figure 2.11. The quantizer is preceded by a block called *loopfilter*, the output of the quantizer $y[n]$ is connected to a digital-to-analog converter (DAC). Its output is then fed back to the input, where is subtracted

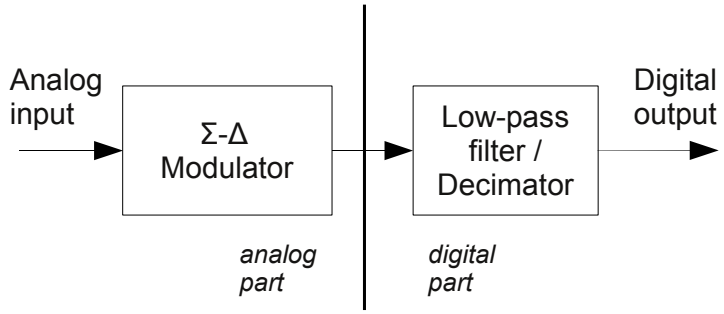


Figure 2.10: Sigma-Delta analog-to-digital converter diagram

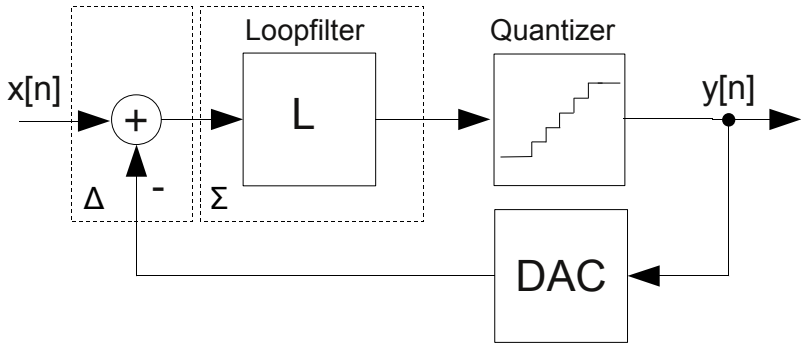


Figure 2.11: Basic scheme of a sigma-delta modulator

from the input signal $x[n]$ and this difference serves as input to the loopfilter. In general, the loopfilter is designed to have high gain in the frequency band of interest and strong attenuation outside this band, as consequence, the in-band quantization noise is strongly attenuated.

The loopfilter illustrated in figure 2.11 can contain one or more integrators. The order of the Σ-Δ modulator is given by the number of integrators inside the loopfilter, i.e., a first order Σ-Δ modulator contains one integrator in the loopfilter. The system of figure 2.11 can be increased by adding more cascade loopfilters in order to obtain higher order modulator and therefore to increase the process of noise shaping [4]. The Greek letters Σ and Δ in the nomenclature of the modulator refer to the modulation process: first the subtraction (Δ) of the input with the last output and then, the summation (Σ) in the loopfilter.

2.3.2 First Order Σ-Δ Modulator

The first order Σ-Δ modulator has one integrator in the loopfilter, a 1-bit quantizer and a 1-bit DAC in the feedback loop as illustrated in figure 2.12.

Assuming an ideal integrator, an ideal 1-bit quantizer and a perfect operation of the

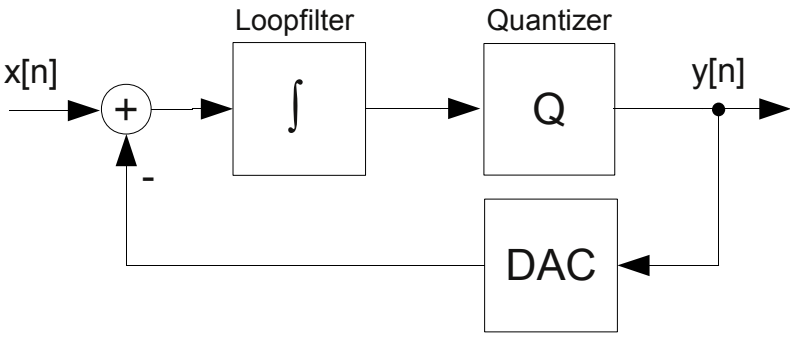


Figure 2.12: Block diagram of a first order sigma-delta modulator

DAC. Replacing the quantizer by its linear model, the output signal $y[n]$ is

$$y[n] = x[n] + e[n] - e[n-1]. \tag{2.15}$$

Applying the z-transform [17] to equation (2.15) the output of the modulator in the z-domain becomes:

$$Y(z) = X(z) + \left(1 - z^{-1}\right) E(z), \tag{2.16}$$

and the z-domain model of the first order modulator is depicted in figure 2.13 A more

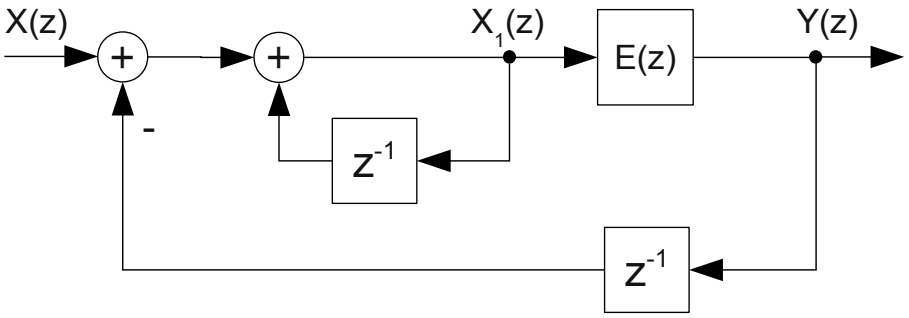


Figure 2.13: Z-domain model of a first order sigma-delta modulator

general expression to represent the modulator model is [4]:

$$Y(z) = STF(z) X(z) + NTF(z) E(z), \tag{2.17}$$

where $STF(z)$ is called the Signal Transfer Function and $NTF(z)$ is called the Noise Transfer Function. In this case the $STF(z)$ is equal to 1 and the $NTF(z)$ is equal to $(1 - z^{-1})$.

The last term in equation (2.16) is a filtered version of the quantization noise $Q(z) = (1 - z^{-1}) E(z)$. In order to quantify the filtering process of the sigma-delta modulator, is useful to find the *Power Spectral Density* (PSD) of $Q(z)$. By setting $z = e^{j2\pi \frac{f}{f_s}}$ the

PSD is

$$S_q(f) = \underbrace{\left[2\sin\left(\pi\frac{f}{f_s}\right)\right]^2}_{\left[NTF\left(e^{j2\pi\frac{f}{fs}}\right)\right]^2} S_e(f), \tag{2.18}$$

where f_s is the sampling rate and $S_e(f)$ is the 1-sided PSD of the quantization noise $e[n]$.

Figure 2.14 depicts the frequency response of the NTF. It is clear to see that the NTF has a high-pass frequency response, therefore the quantization noise is attenuated at lower frequencies while it is amplified at higher frequencies.

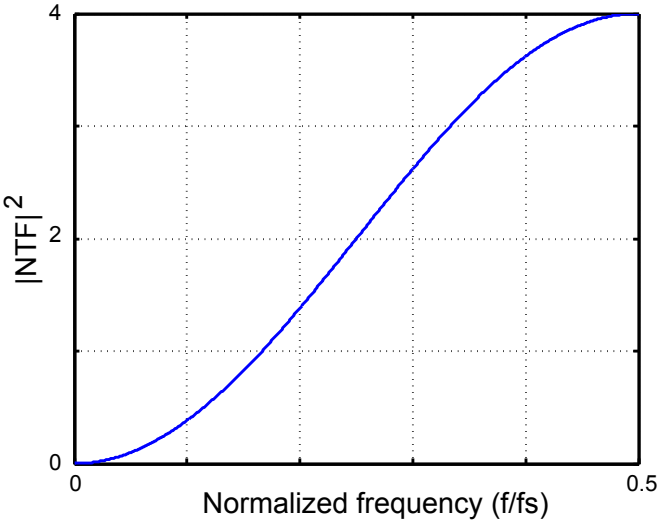


Figure 2.14: Frequency response of the Noise Transfer Function of a first order sigma-delta modulator

This filtering process is named *noise shaping*, and it is the main advantage of the sigma-delta modulation. Since the Σ-Δ modulation is based on oversampling, the frequency band-of-interest is close to *zero frequency* where the amount of quantization noise is reduced by the filtering process of the NTF of the modulator. Thus, the *oversampling ratio* (OSR) can be introduced as the ratio between the maximum input signal frequency f_B and the frequency $f_s/2$

$$OSR = \frac{f_s}{2f_B}. \tag{2.19}$$

Integrating S_q between 0 and f_B, an approximated value of the noise power σ_q^2, in the frequency band of interest, can be obtained. Assuming OSR $\gg 1$:

$$\sigma_q^2 = \int_0^{f_B} S_q(f)\, df \approx \frac{\pi^2\sigma_e^2}{3(OSR)^3}. \tag{2.20}$$

As expected, increasing the OSR decreases the in-band noise. Using equation (2.11)

in combination with equation (2.20) the SNR in dB is

$$SNR = 20\log\left(\frac{\sigma_s}{\sigma_e}\right) + 10\log\left(\frac{3}{\pi^2}\right) + 30\log(OSR). \tag{2.21}$$

Therefore, doubling the OSR in a first order Σ-Δ modulator increases the signal-to-noise ratio by 9 dB and the effective number of bits is increased by 1.5 bits (see equation (2.14)).

2.3.3 Second Order Σ-Δ Modulator

The second order Σ-Δ modulator can be constructed adding another integrator and a feedback path to the first order Σ-Δ modulator as shown in figure 2.15.

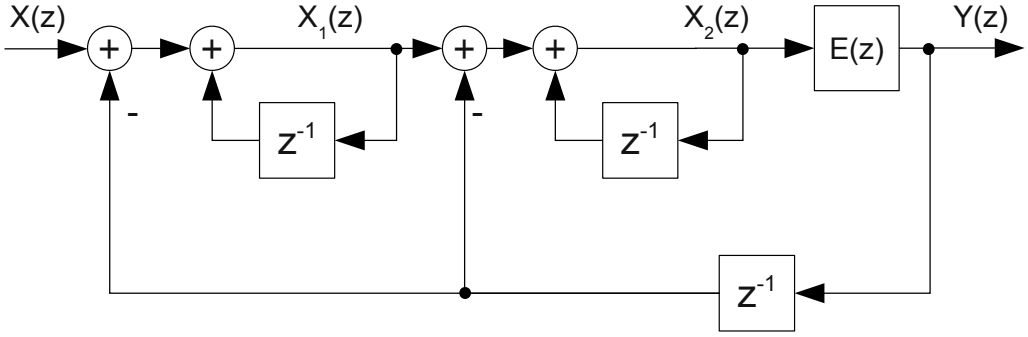


Figure 2.15: Second order Σ-Δ modulator

In the z-domain, the linear model for the second order Σ-Δ modulator can be obtained using the additive noise model for the quantizer (see figure 2.7) and is depicted in figure 2.16.

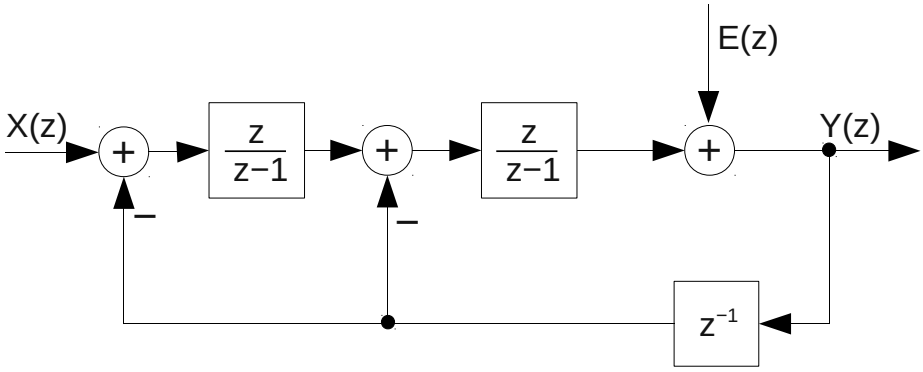


Figure 2.16: Z-domain linear model of a second order sigma-delta modulator

Doing the same analysis as for the first order Σ-Δ modulator, the output $Y(z)$ of the linear model is:

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^2 E(z). \tag{2.22}$$

As for the first order modulator, the $STF(z) = 1$, but now the $NTF(z) = (1 - z^{-1})^2$ is the first order NTF squared, thus the attenuation at lower frequencies of the quantization noise increases.

Following the same steps as for the first order modulator, the noise power in the frequency band of interest can be estimated as

$$\sigma_q^2 = \int_0^{f_B} S_q(f)\, df \approx \frac{\pi^4 \sigma_e^2}{5(OSR)^5}. \tag{2.23}$$

In comparison with the in-band noise power of the first order modulator, doubling the OSR increases the SNR by 15 dB and hence the effective resolution is increased by 2.5 bits. A visual comparison of both noise transfer functions is presented in figure 2.17.

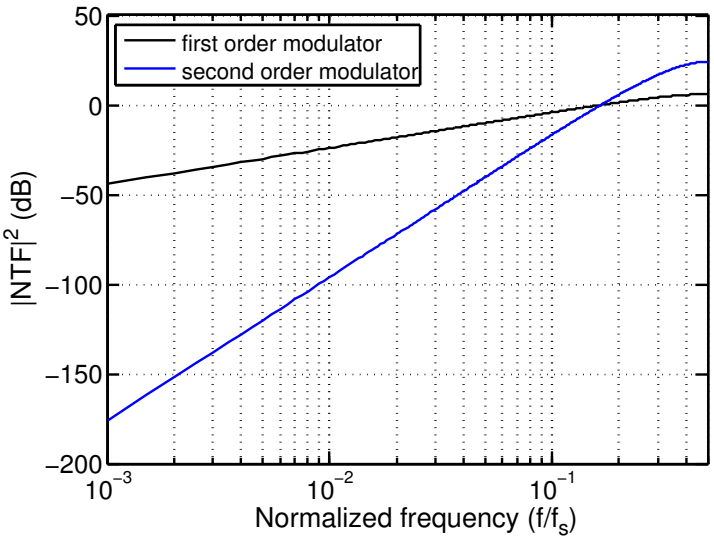


Figure 2.17: Comparison of the first and second order Noise Transfer Functions

2.3.4 Other Second Order Structures

Other structures for a second order modulator exist [4]. A useful structure, which is used in the ADC [23] of this work, is the Silva-Steensgaard modulator [4, 24, 25] shown in figure 2.18. Its main features are:

1. the circuit has a feed-forward path from the input to the quantizer,
2. the feedback signal to the input only contains the shaped quantization noise,
3. the second integrator delivers a delayed quantization noise signal which can be used as input to a next modulator in multi-stage structures.

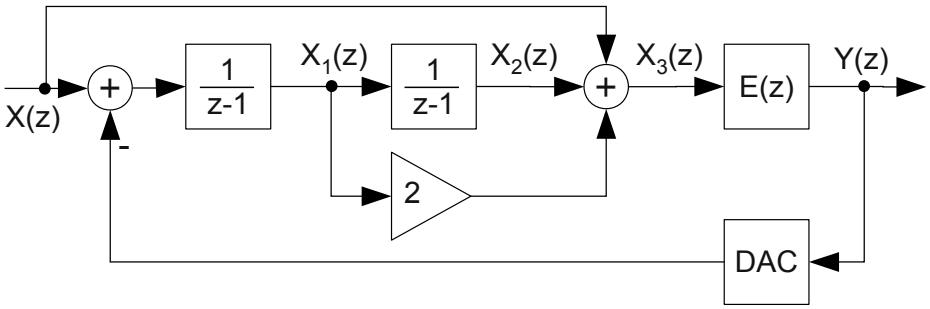


Figure 2.18: Silva-Steensgaard second order sigma-delta modulator

The modulator output $Y(z)$ is

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{2.24}$$

again the $STF = 1$ and the $NTF = (1 - z^{-1})^2$.

The output of the first integrator $X_1(z)$ is

$$X_1(z) = -\left(1 - z^{-1}\right) z^{-1} E(z). \tag{2.25}$$

The output of the second integrator $X_2(z)$ is

$$X_2(z) = -z^{-2} E(z) \tag{2.26}$$

which is the quantization noise $E(z)$ delayed by two samples. Then, $X_2(z)$ can be used as input for noise cancelling topologies [4].

And, the input to the quantizer $X_3(z)$ is

$$X_3(z) = X(z) + 2X_1(z) + X_2(z) = X(z) - z^{-1}\left(2 - z^{-1}\right) E(z). \tag{2.27}$$

2.3.5 Multi Stage Σ-Δ Modulator

To increase the SNR, and thus the effective resolution, by means of raising the modulator order is only possible to a certain level due to stability and dynamic range considerations. Owing to this reason a different strategy, based on noise cancellation instead of noise filtering, is adopted.

Noise cancellation is accomplished by using multiple stages cascaded systems for the modulator −known as multi-stage noise-shaping (MASH)− [4]. A 3-stage cascading system is depicted in figure 2.19.

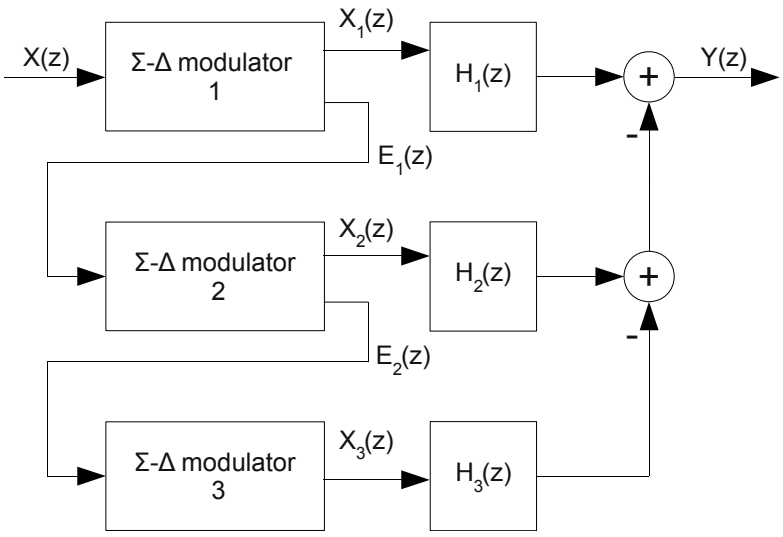


Figure 2.19: 3-stage MASH topology block diagram

The output $X_1(z)$ of the first modulator is

$$X_1(z) = STF_1(z)X(z) + NTF_1(z)E_1(z), \tag{2.28}$$

where $STF_1(z)$ and $NTF_1(z)$ are the signal transfer function and noise transfer function, respectively, of the modulator 1. As shown in figure 2.19, the quantization noise $E_1(z)$ of the first stage is fed to the second stage, modulator 2. Doing the same analysis for the second stage its output $X_2(z)$ can be written as:

$$X_2(z) = SFT_2(z)E_1(z) + NTF_2(z)E_2(z). \tag{2.29}$$

Also, the quantization noise of the second stage $E_2(z)$ is fed to the next stage and thus, the output $X_3(z)$ of the third stage can be expressed as:

$$X_3(z) = SFT_3(z)E_2(z) + NTF_3(z)E_3(z), \tag{2.30}$$

and the output $Y(z)$ becomes:

$$\begin{aligned} Y(z) &= H_1(z)\left[STF_1(z)X(z) + NTF_1(z)E_1(z)\right] \\ &- H_2(z)\left[STF_2(z)E_1(z) + NTF_2(z)E_2(z)\right] \\ &+ H_3(z)\left[STF_3(z)E_2(z) + NTF_3(z)E_3(z)\right]. \end{aligned} \tag{2.31}$$

The filters $H_1(z)$, $H_2(z)$ and $H_3(z)$ are designed to cancel the quantization noise of

the overall process. The cancellation conditions [4] are

$$\begin{aligned} H_1(z)NTF_1(z) - H_2(z)STF_2(z) &= 0 \\ H_2(z)NTF_2(z) - H_3(z)STF_3(z) &= 0. \end{aligned} \tag{2.32}$$

Under these constraints $E_1(z)$ and $E_2(z)$ are cancelled, thus the output $Y(z)$ becomes

$$Y(z) = STF_1(z)H_1(z)X(z) + NTF_3(z)H_3(z)E_3(z). \tag{2.33}$$

Using equation (2.32) to find $H_3(z)$, the output $Y(z)$ can be rewritten as

$$Y(z) = STF_1(z)H_1(z)X(z) + \left(\frac{H_1(z)NTF_1(z)NTF_2(z)NTF_3(z)}{STF_2(z)STF_3(z)}\right) E_3(z). \tag{2.34}$$

Therefore, under ideal conditions, the quantization noise of the first two stages is cancelled, while the quantization noise from the third modulator is filtered by the product of the three NTF's.

The main advantages of the topology are:

- the remaining error at the output is the quantization error $E_3(z)$ filtered by the product of the three noise transfer functions,
- it often allows to use multi-bit quantizers in the intermediate stages,
- no harmonic distortion of the input signal is generated in the intermediate stages, since the input of the intermediate stages contains quantization noise rather than the input signal.

However, the quantization noise cancellation is not perfect due to mismatches between the transfer functions of the modulators $NTF_k(z)$, $STF_k(z)$ and the transfer functions of the digital filters $H_k(z)$. As a consequence, the theoretically predicted SNR performance cannot be achieved.

Generally, ADCs of this topology are designed using second order modulators. Thereby the noise performance of a fourth order modulator can be achieved using second order modulators without the stability problems present in high order modulators. A complete coverage of this topic can be found in reference [4].

2.3.6 Decimation Filters

As has been presented, the main characteristic of a Σ-Δ modulator is to attenuate the quantization noise at low frequencies. This attenuation however amplifies the quantization noise at high frequencies (see figures 2.14 and 2.17).

To be useful as ADCs, the out-of-band noise has to be removed by digital filtering, then the filtered output signal has to be *downsampled* or *decimated* [17, 22] to the Nyquist sampling frequency $2f_B$, where f_B is the highest frequency component to be sampled by the ADC. The requirements are a digital low-pass filter (LPF) with a nearly flat frequency response in the signal band [0,f_B] and a high attenuation in the band (f_B, $f_s/2$]. In general these are satisfied by using low-pass digital filters implemented as Sinc, brick-wall, comb or finite impulse response (FIR) [22].

Usually more than one filter stage is used, commonly between two or three stages, depending on the resolution requirements [4]. The decimation process is stated in figure 2.20 for a two-stage approach.

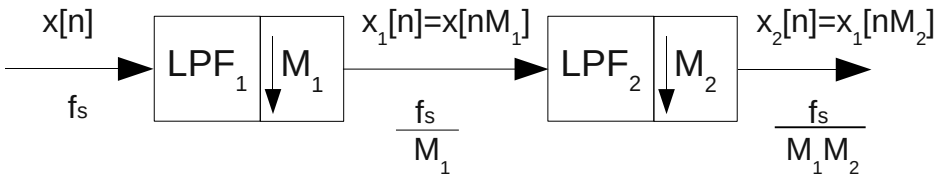


Figure 2.20: A two-stage decimation filter

The decimation process can be described as follows: the input signal or sequence $x[n]$ enters the first stage at a frequency equal to f_s, where it is filtered by the low-pass filter LPF_1 in order to avoid aliasing and then it is *"re-sampled"* at a frequency $f_1 = f_s/M_1$. The new output sequence is

$$x_1[n] = x[nM_1]. \tag{2.35}$$

This new sequence $x_1[n]$ reaches the second stage where it is filtered by the low-pass filter LPF_2 to prevent aliasing, and re-sampled at a sampling rate $f_2 = f_1/M_2$. Therefore, the new output sequence $x_2[n]$ is a representation of the input sequence $x[n]$ at a lower sampling rate $f_2 = \dfrac{f_s}{M_1 M_2}$ or

$$x_2[n] = x_1[nM_2] = x[nM_1M_2]. \tag{2.36}$$

As a consequence of the decimation process the output $x_2[n]$ has a bandwidth M_1M_2 lower than the original bandwidth of $x[n]$, as expressed by the relation

$$f_2 = 2f_B = \frac{f_s}{M_1M_2}. \tag{2.37}$$

Then, $OSR = M_1M_2$. Figure 2.21 illustrates the decimation filters effects on a first order Σ-Δ modulator. The output signal bandwidth is reduced to f_B. The in-band quantization noise is attenuated by the filtering process, as shown in the shadowed area in figure 2.21.

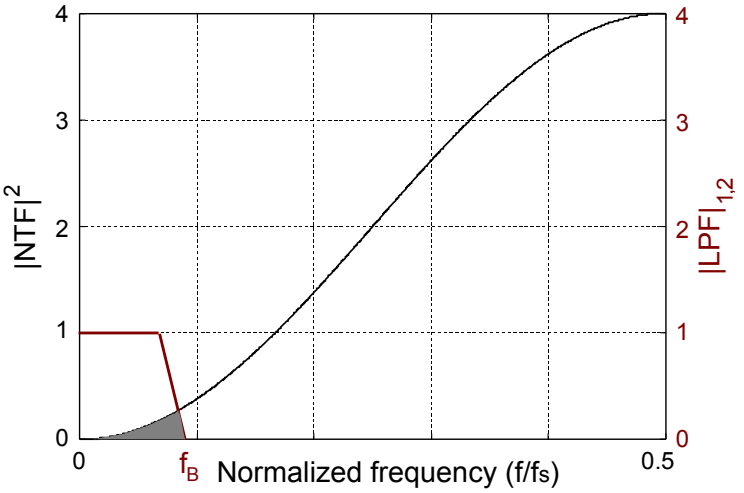


Figure 2.21: Example of a decimation process on the Noise Transfer Function

2.4 The Sigma-Delta ADC Used in this Thesis

The internal configuration of the Σ-Δ ADC used in this thesis is depicted in Figure 2.22. It consists of a 3-stage (2-2-0) MASH architecture (the numbers in parentheses refer to the orders of the individuals modulators).

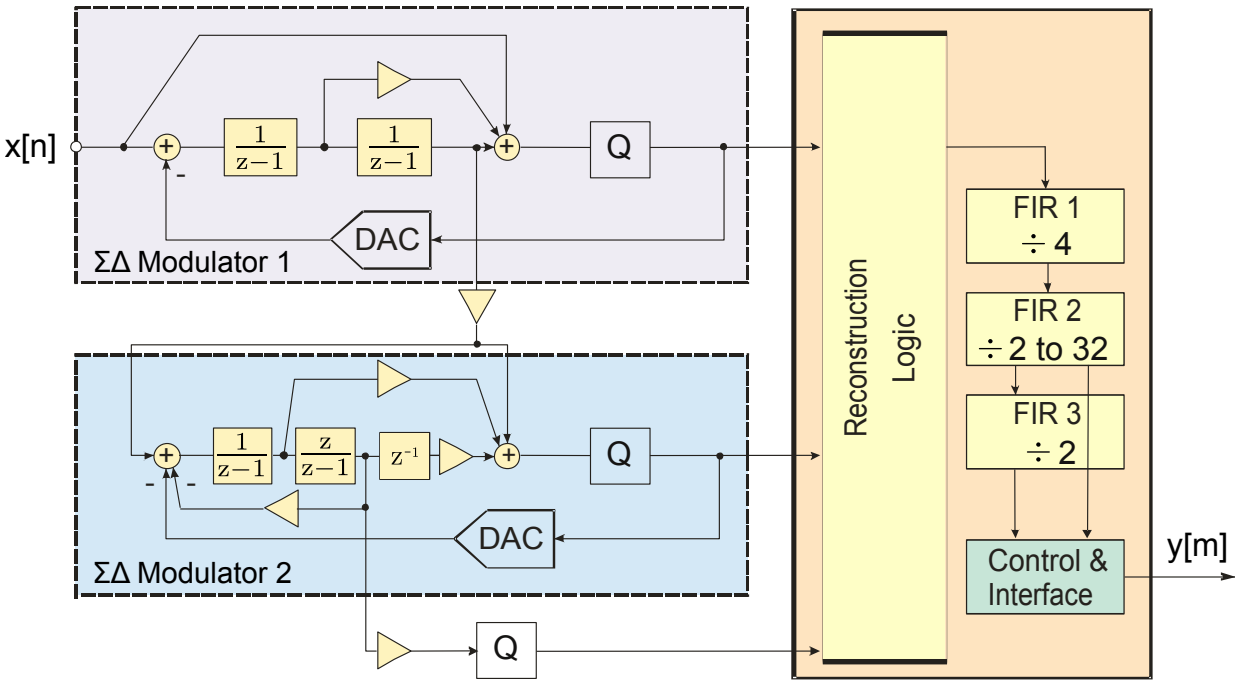


Figure 2.22: Internal structure of the Σ-Δ ADC from [23]

The first and second stages employ feed-forward topology based on the Silva-Steensgaard structure. The second stage is also based on the same structure but the designers have spread the zeros of the NTF in order to minimize the quantization noise when setting a

lower OSR. And, the third stage is a flash ADC [23].

The Σ-Δ ADC has a 3-stage decimation filter. The first stage reduces the sampling rate by 4. The second stage can be programmed to reduce the sampling rate even further, from 2 to 32. And, the third stage can be bypassed or reduces the sampling rate further by 2. As consequence, programming the maximum decimation rate for all decimation filter an OSR = 256 can be achieved. In addition, the coefficients of the decimation filter of the third stage can be programmed by the user.

Chapter 3

System Description

This chapter describes the different modules of the sampling system. The performance of the system is limited by the accuracy and deviations of its components, thus a description of how these deviations introduce errors in the overall system performance are illustrated. Finally, the spectrum of a sampled signal is presented which shows the influence of the system elements to the overall performance.

3.1 Sampling System Description

Sigma-Delta analog-to-digital converters have recently become more attractive for high precision sampling applications due to their improved characteristics, such as: low-noise, high resolution and low non-linearity [4]. A previous evaluation of such a device, carried out at PTB, confirmed their feasibility for high-grade metrology applications [5, 26]. As a result, a sampling system based on Σ-Δ ADC has been designed, which incorporates the expertise obtained in such investigations. This system is made up of six main modules, i) the input buffer, ii) the fully differential amplifier plus anti-aliasing filter, iii) the ADC, iv) the voltage reference, v) the sampling clock and vi) the ADC control unit. Figure 3.1 depicts the block diagram of the sampling system and a photograph of the front view of the sampling system is shown in figure 3.2. Each module is described in the following sections.

3.1.1 Sigma-Delta Analog-to-Digital Converter

The sampling system is based on a commercially available Σ-Δ ADC with 24-bit resolution, the AD7763 designed by Analog Devices [27]. Its main characteristics are: 1) it uses a multibit Σ-Δ modulator, 2) it has a wide bandwidth up to 250 kHz, 3) it has a cascade of three stages low-pass digital finite impulse response (FIR) filters with programmable

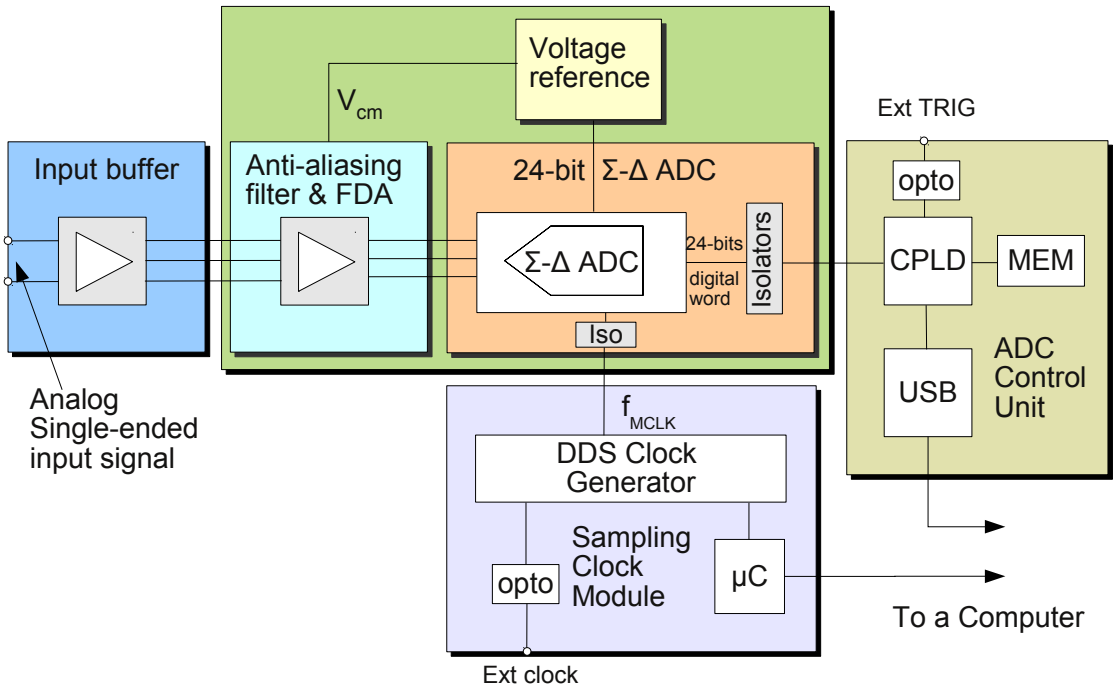


Figure 3.1: Sampling system block diagram composed by: i) Input buffer, ii) Anti-aliasing filter and fully differential amplifier (FDA), iii) 24-bit Σ-Δ ADC, iv) Voltage reference, v) Sampling clock module, and vi) ADC control unit.

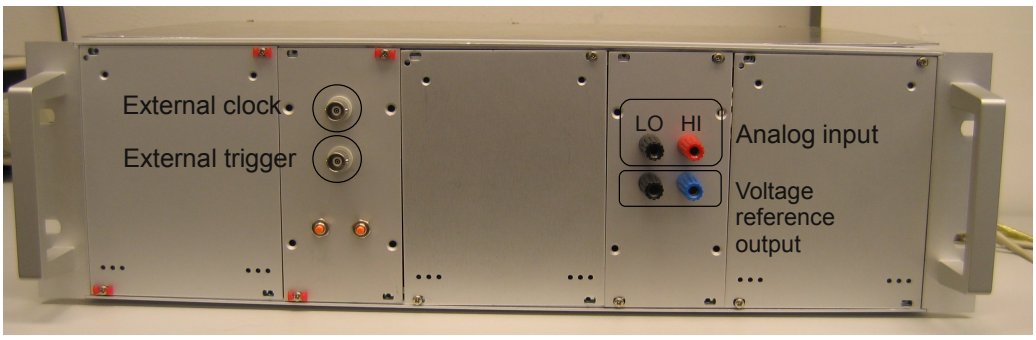


Figure 3.2: Σ-Δ sampling system front view

decimation rates from 32 to 256. The last filter stage coefficients can be programmed by the user or left with the default coefficients. 4) The achievable SNR is 112 dB at an equivalent sampling rate of 78 kHz and a decimation rate of 256 (this is equivalent to a Nyquist data converter of 18 bit resolution), 5) the modulator input is fully differential and 6) the digital output front-end is serial allowing the synchronization of multiple devices [27].

The ADC input range is determined by the voltage reference. For example, with a voltage reference of nominal value 4.096 V, the ADC input range is 1.6384 V peak around a common-mode voltage of 2.048 V [27].

The ADC was mounted on a four layer printed circuit board (PCB) following the rec-

ommendations given by the manufacturer in order to reach high resolution and accuracy. The PCB was divided into four sections: i) the analog input and the ADC, ii) the voltage reference, iii) the clock signal input and iv) digital signals and interface. The ADC and analog input share a ground plane. Two separated ground areas were destined for the digital interface and the clock signal input. Figure 3.3 shows a photograph of the four layer PCB.

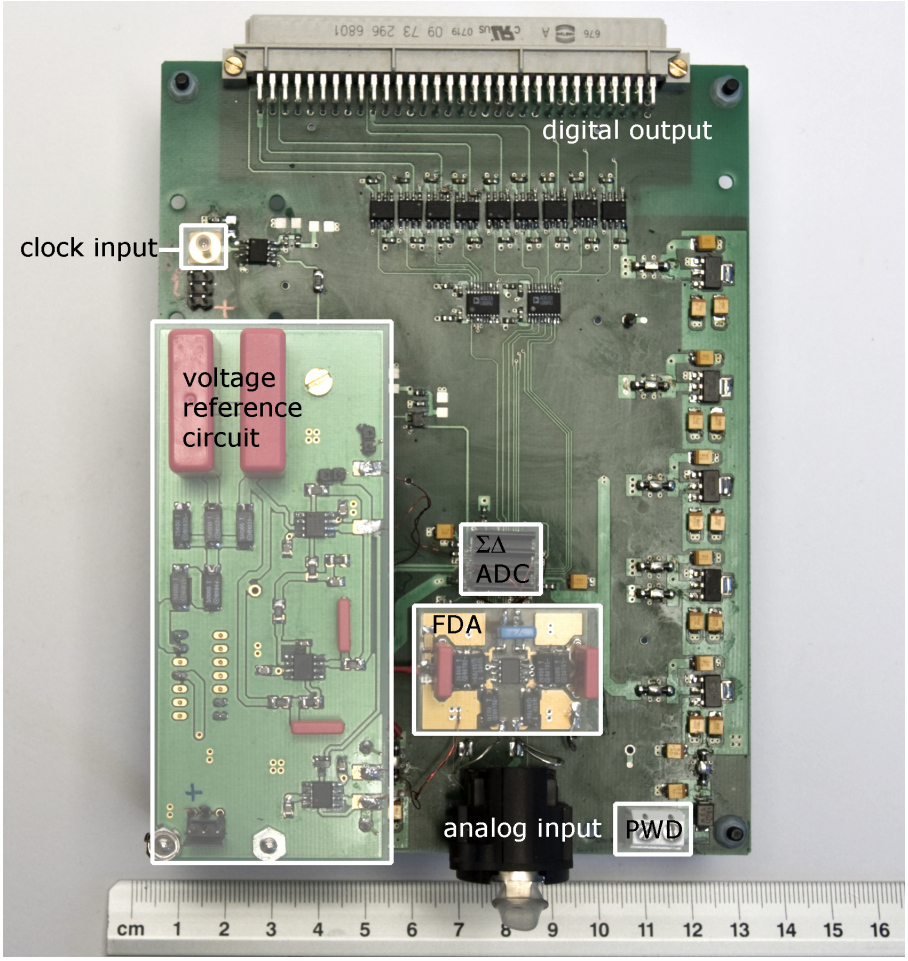


Figure 3.3: Photograph of the PCB of the ADC. The main parts are labeled: the Σ-Δ ADC, the voltage reference circuit, the fully differential amplifier (FDA), the clock signal input, the digital output and the analog input

The voltage reference circuitry was mounted on an external two layer PCB in order to decouple interference and noise from the ADC. This PCB was piggybacked close to the ADC voltage reference input pin as shown in figure 3.3.

Additionally, to avoid coupled interference from the digital circuits, digital signal isolators were used on the sampling clock input, data and status outputs of the ADC chip.

The schematic circuits of the Σ-Δ ADC are depicted in figure B.1 to figure B.4.

3.1.2 Fully Differential Amplifier and Anti-aliasing Filter

The ADC input stage requires a positive fully differential signal. As a consequence, a previous stage is needed to adjust the signal amplitude to the ADC input voltage, to shift the DC level of the input signal to the common voltage required by the ADC (usually the half of the voltage reference) and to filter the signal to avoid aliasing. This signal conditioning can be performed by means of a fully differential amplifier.

A fully differential amplifier (FDA), the THS-4521 from Texas Instrument [28] was used for conditioning the output differential signal of the input buffer to the requirements of the Σ-Δ input modulator. Figure 3.4 shows the schematic circuit of the FDA and the PCB is illustrated in figure 3.3 labeled as FDA. First, the gain of the FDA was set to a nominal value of 0.4, so that the signal was attenuated to have an input range of ±2.048 V (FSR=4.096 V). High precision surface mounted resistors were used for this purpose [29]. Then, the signal was shifted to positive values centering them at the half of the voltage reference value (2.048 V). Therefore, the common mode voltage (V_{CM}) input pin of the FDA was connected to the corresponding $V_{ref}/2$ output of the voltage reference circuitry.

The FDA was also configured as a low-pass filter by adding a capacitor C_f in parallel with the feedback resistor R_f, as depicted in figure 3.4. The cut-off frequency of this filter is 398 kHz. A second low-pass filter was added at the output of the FDA formed by R_s and C_s, the cut-off frequency of this filter is 2.65 MHz. As a result, both filters conform a double real pole low-pass filter. In addition, the resistor R_s also isolates the FDA from the capacitive load of the ADC input stage.

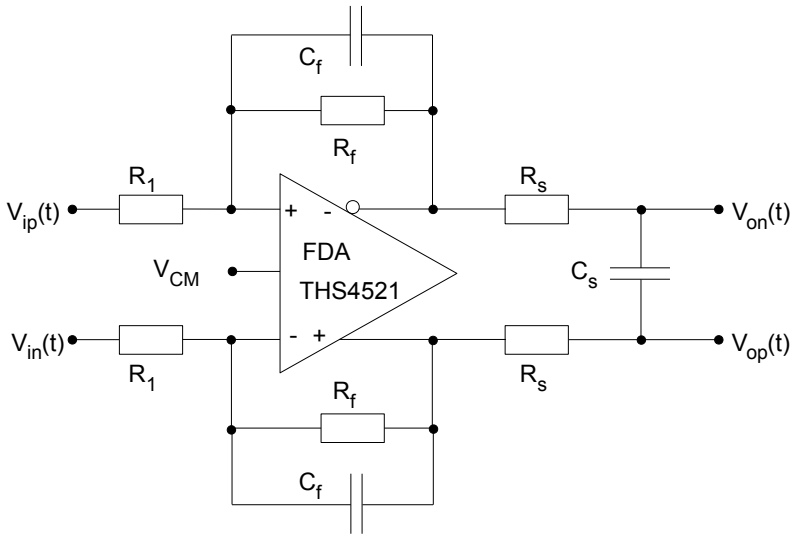


Figure 3.4: Block diagram of the fully differential amplifier

Differential signals have some advantages over unipolar signals, such as: a) the immunity to noise is increased provided that the transport wires and paths are kept as short as

possible, b) because of the change in phase of the output differential, the dynamic range is increased by a factor of 2 over a single-ended output for the same voltage swing, c) a differential output ideally removes even harmonic products introduced by the amplifier. A general introduction to fully differential amplifiers can be found in reference [30] and for the special application on this thesis in references [31, 32]. The electrical circuit is depicted in figure B.6.

3.1.3 Input Buffer

The system was designed to sample single-ended bipolar signals. As introduced in the previous sections the ADC requires a positive differential signal. The level conditioning is performed by the FDA as described above. Sometimes, the performance of such amplifiers is not good enough for high accuracy application and a prior signal conditioning stage is required. Consequently, an input buffer was included.

The single-ended bipolar signal at the input of the system to be sampled is converted to a differential signal by means of an input buffer with nominal gain ± 1. This differential output signal of the input buffer is then fed to a fully differential amplifier for scaling, anti-aliasing filtering and DC level shifting, and further directed to the Σ-Δ modulator input.

The input buffer is a cascade of two amplifiers. The first stage is a follower amplifier (G=1) and the second stage is an inverter amplifier (G=-1). Both of them are *composite amplifiers*, as detailed below. Figure 3.5 shows a simplified block diagram of the input buffer. Figure 3.6 illustrates the PCB.

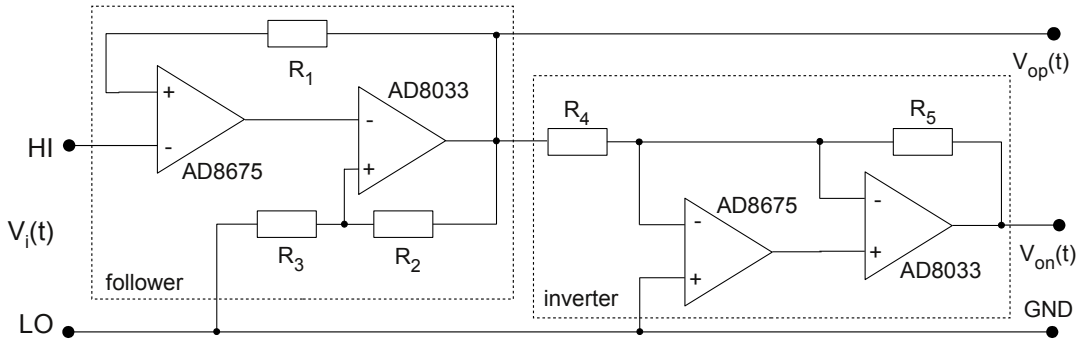


Figure 3.5: Simplified block diagram of the input buffer

Composite amplifiers are preferred in high precision applications because, in general, a single operational amplifier is not enough to accomplish high performance. A composite amplifier is made up of two (or more) operational amplifiers so that the performance of the amplifiers are combined. For example, one operational amplifier with very good input characteristics (high precision, low noise, low offset) is combined with another operational

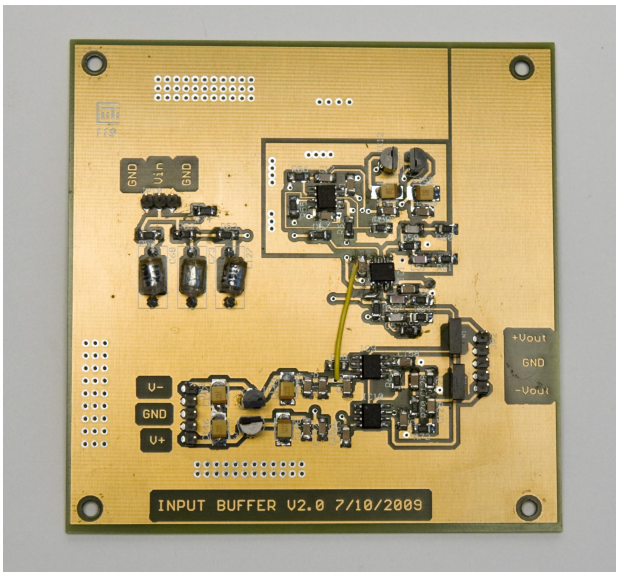


Figure 3.6: Input Buffer PCB

amplifier with very good output characteristics (high speed, high power) [33, 34]. The input buffer combined the good DC characteristics of the operational amplifier AD8675 [35] with the good AC characteristics of the AD8033 [36].

Another important characteristic is the input impedance of the system. The input impedance of the FDA circuit is 1 kΩ. Owing to this low input impedance may produce a loading error, the input buffer increases the input impedance of the system to 10 MΩ minimizing this loading error.

3.1.4 Voltage Reference

The ADC converts a continuous-time signal to a discrete-time signal by comparing the input signal voltage at a time $t = T_s$, T_s sampling time, with the voltage value of its voltage reference. Therefore, the performance of the voltage reference is one of the main limitations in the overall system performance, due to the fact that the accuracy of the conversion process is determined by the accuracy of the voltage reference. As a consequence, a low-noise and low-drift voltage reference was selected, the VRE105CA from Thaler Corporation [37].

The voltage reference circuit was composed of a resistive voltage divider with three surface mounted resistors (series SMR1D [29]) to reduce the output voltage from 5 V to 4.096 V as required by the ADC. A low pass filter with a cut-off frequency of 7 Hz is added to reduce the low frequency noise of the voltage reference integrated circuit (IC). This filter is a bootstrapping configuration in order to reduce errors due to leakage current as described in reference [38]. Figure 3.7 shows a block diagram of the voltage reference

circuit and the voltage reference PCB can be seen at the lower left corner of figure 3.3.

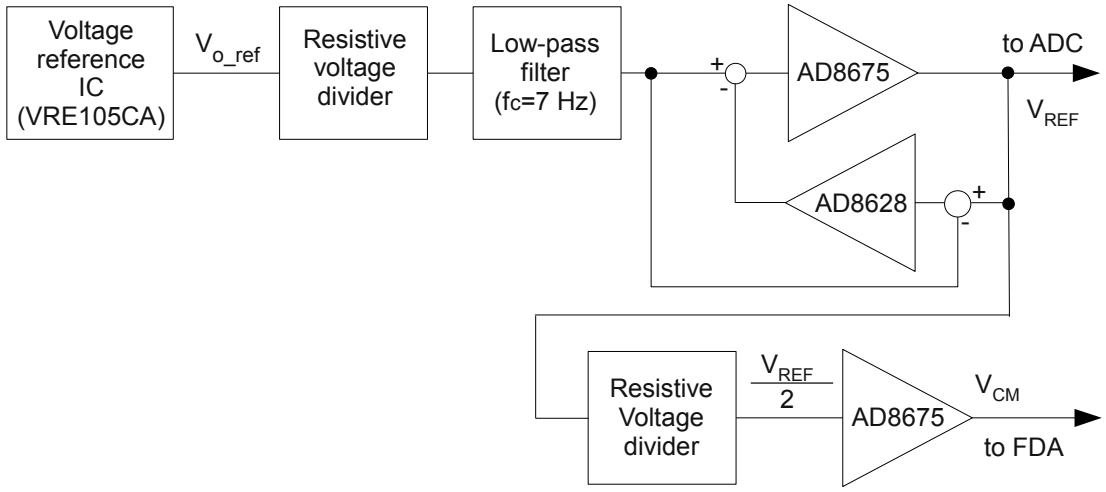


Figure 3.7: Block diagram of the voltage reference circuit

A buffer was added at the output of the low-pass filter in order to deliver current to the ADC and to avoid loading the voltage reference IC directly. A low-noise operational amplifier, the AD8675 [35] is used. A zero-drift operational amplifier, the AD8628 [39], stabilizes the thermal drift of the AD8675.

The circuit has an additional output to provide the common mode voltage $V_{CM}=\frac{V_{ref}}{2}$ to the FDA. For this purpose, an integrated resistive voltage divider of two resistors with equal nominal values 10 kΩ and a zero-drift buffer were included. The schema of the electrical circuit is illustrated in figure B.5.

3.1.5 Sampling Clock Module

The ADC requires an external, low time jitter clock signal. Therefore, the system was provided by an external clock module based on Direct Digital Synthesis [40]. The particular module used in this thesis was based on reference [41] where a commercial Direct Digital Synthesizer (DDS) device was studied as clock source for sampling systems.

The sampling clock module employs a Direct Digital Synthesizer (DDS) to provide the sampling clock frequency f_{MCLK} to the Σ-Δ ADC. The DDS output frequency is set by a microcontroller from 1 MHz to 20 MHz with a resolution of 48-bits which is equivalent to a resolution in frequency of $\approx 0.5\,\mu$Hz.

The requirements of the sampling clock are stability in frequency and low time jitter. The maximum allowable time jitter for an oversampling ADC is given by [27]:

$$t_{j(rms)} \leq \frac{\sqrt{OSR}}{2\pi \cdot f_{IN} \cdot 10^{\frac{SNR(dB)}{20}}} \tag{3.1}$$

where: OSR is the oversampling ratio, SNR is the target signal-to-noise ratio and f_{IN} is the maximum signal frequency. For instance, input signals up to 2 kHz are sampled with a target SNR = 120 dB and OSR = 256, the time jitter has to be:

$$t_{j(rms)} \leq \frac{\sqrt{256}}{2\pi \cdot 2000 \cdot 10^{\frac{120}{20}}} = 1.27 \quad \text{ns}$$

For the device used in this thesis, the AD9852 from Analog Devices [42], the peak-to-peak time jitter has been measured to be less than 400 ps [41]. The PCB of the clock module is depicted in figure 3.8.

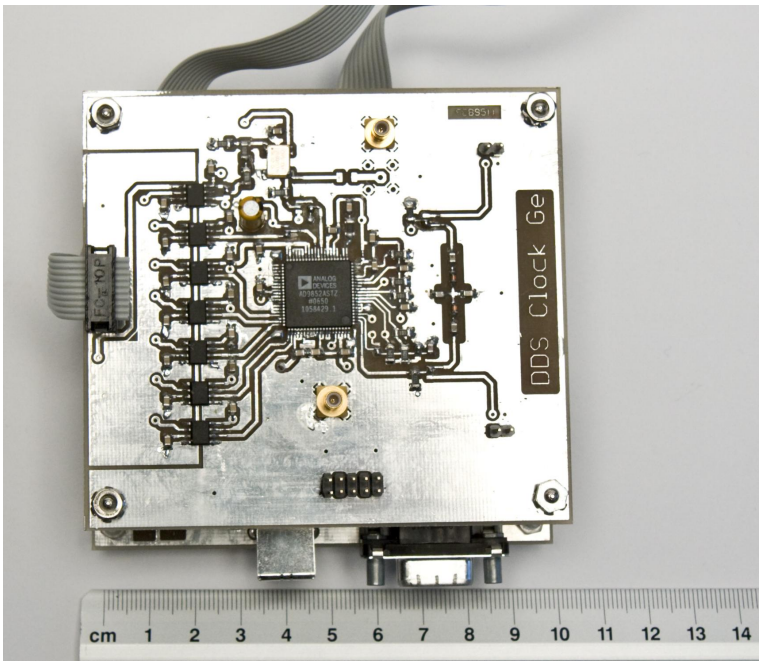


Figure 3.8: Sampling clock module PCB. The layout and the circuit were based on reference [41]

In high performance and high accuracy applications it is of utmost importance to synchronize the sampling system with the signal generator to be measured as described in [43] in order to fulfill the conditions for coherent sampling and to avoid spectral leakage when computing the discrete Fourier transform on the sampled data, i.e. $\frac{f_s}{f} = J$ with J a positive integer number, where f_s is the sampling rate and f is the signal frequency. Thus, an optical coupler was added to provide the system with an external clock input to allow synchronization.

3.1.6 Σ-Δ ADC Control Unit

The ADC readouts have to be sent to a personal computer for further processing and analysis. To accomplish this task a universal hardware was included to gather the ADC data, to store them in a buffer prior to be sent to computer, and to configure the ADC. This hardware was previously designed for such applications and is described in reference [44]. A photograph of the ADC Control Unit is shown in figure 3.9.

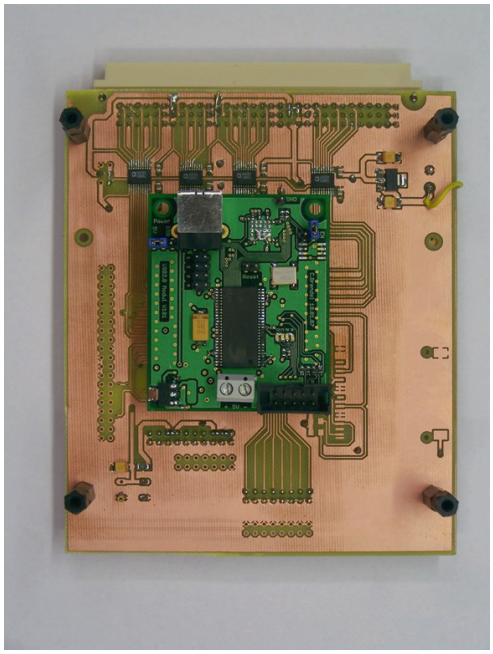


Figure 3.9: Σ-Δ ADC Control Unit. The USB-Modul hardware from reference [44] and the adapter to connect the ADC PCB to the USB-Modul

The Σ-Δ ADC control unit was programmed in Verilog hardware description language (Verilog-HDL) on a complex programmable logic device (CPLD) and consists of three state machines. One state machine converts the Σ-Δ ADC's data stream from serial to parallel and stores the data stream in the memory buffer (MEM on figure 3.1) before being sent to the host computer over USB for further analysis. The memory buffer allows storing up to 524288 samples, each of them of 32 bits long. A second state machine outputs the sampled data through a universal-serial bus interface (USB). At start-up, the third state machine configures the Σ-Δ ADC decimation rate to the maximum value of 256 and the operating mode to normal mode with which the best performance of the ADC is achieved [27].

3.2 Sources of Errors

Any deviations and/or mismatches on the components of the different modules, such as amplifiers, resistors, capacitors, may degrade the performance and accuracy of the sampling system. These deviations and/or mismatches are considered as source of errors and are described in this section.

The main sources of errors in the system are located in:

- the input buffer and the fully differential amplifier,
- the Σ-Δ ADC,
- the voltage reference and
- the sampling clock module.

3.2.1 Sources of Errors in the Input Buffer and Fully Differential Amplifier

In amplifiers, errors are classified in two groups: i) DC and ii) AC errors. DC errors remain constant while AC errors are frequency-dependent. The most important errors of the first group are the input offset voltage and the input bias current. Whereas AC errors degrade the amplifier AC performance such as the common-mode rejection ratio, the open loop gain and the slew rate. Analysis of these errors is well described in the literature and is outside of the scope of this thesis.

In an ideal case, neither the input buffer nor the FDA produce any distortion, therefore the output signals ($V_{op}(t)$) and ($V_{on}(t)$) are balanced in gain and phase. Hence, both of them are equal in amplitude and have a phase shift of exactly π radian as figure 3.10 illustrates.

When designing ADC front-end special considerations have to be taken into account [45, 46]. Mismatches in the circuit components may produce gain and phase deviations between the direct and the inverted signals. These deviations will distort the output signal which is then sampled by the ADC. To illustrate the effects of these deviations consider the input buffer and the FDA as a single stage, as figure 3.11 shows. For simplicity in the analysis a symmetrical third order polynomial transfer function $h(t)$ is considered as

$$h\left(V_i(t)\right) = a_0 + a_1 V_i(t) + a_2 V_i^2(t) + a_3 V_i^3(t). \tag{3.2}$$

If a sinusoidal signal $V_i(t) = A_0 \sin(\omega t)$ is applied to the input, it is converted into a

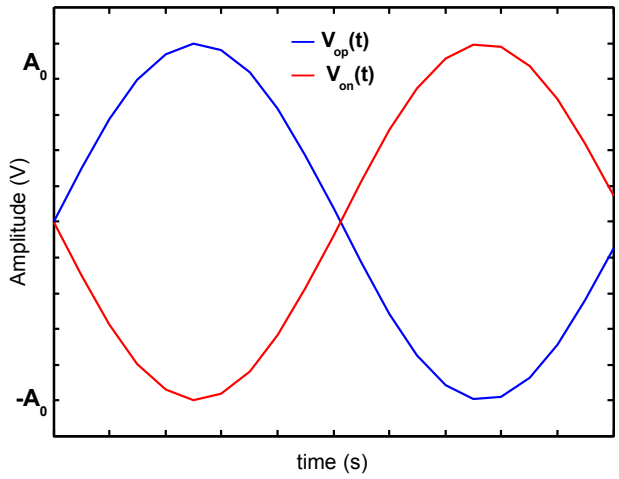


Figure 3.10: Fully differential amplifier ideal case output signal

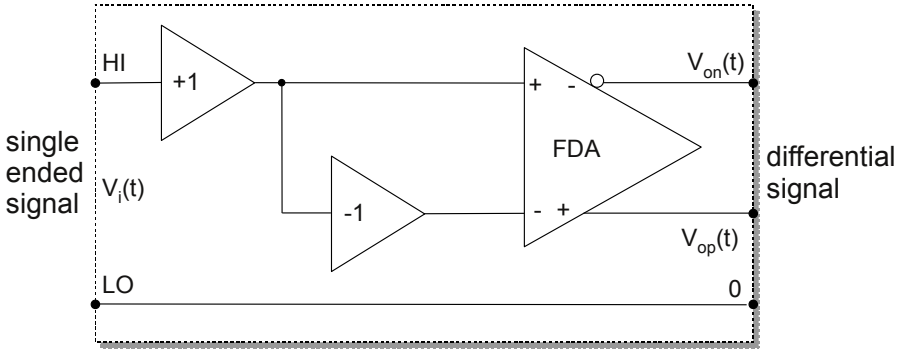


Figure 3.11: Input buffer and fully differential amplifier as a single stage signal conditioning circuitry

pair of signals, $V_{op}(t)$ and $V_{on}(t)$ of the form:

$$V_{op}(t) = G_p\, A_0 \sin(\omega t) \tag{3.3a}$$

$$V_{on}(t) = G_n\, A_0 \sin(\omega t - \pi + \varphi)\,, \tag{3.3b}$$

where $G_p = V_{op}(t)/V_i(t)$ is the non-inverting stage gain and $G_n = V_{on}(t)/V_i(t)$ is the inverting stage gain. Then, the differential output $V_{od}(t)$ is:

$$V_{od}(t) = V_{op}(t) - V_{on}(t) = G_p\, A_0 \sin(\omega t) - G_n\, A_0 \sin(\omega t - \pi + \varphi). \tag{3.4}$$

In the case of gain balance ($G_p = G_n = G$) and phase balance ($\varphi = 0$) the differential output $V_{od}(t)$ becomes:

$$V_{od}(t) = 2\, \sin(\omega t) \left(\frac{3\, a_3\ A^3}{4} + A\, a_1 \right) - \frac{a_3\ A^3 \sin(3\omega t)}{2}\,, \tag{3.5}$$

with $A = G\,A_0$. As equation (3.5) shows, the even order harmonic components are canceled while the odd order harmonic components remain (the third harmonic in this case).

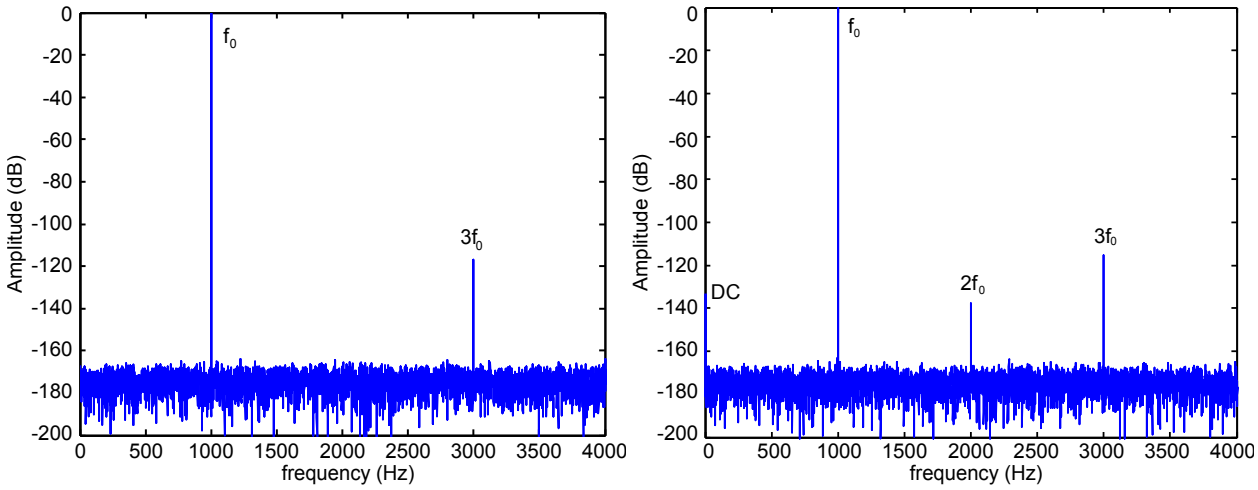
In real cases gain and phase deviations exist. Analyzing the system when there are gain and phase deviations, the differential output $V_{od}(t)$ becomes:

$$\begin{aligned} V_{od}(t) &= \frac{a_2}{2}(A_1^2 - A_2^2) \\ &+ \left(a_1 A_1 + \frac{3}{4}a_3 A_1^3\right)\sin(\omega t) + \left(a_1 A_2 + \frac{3}{4}a_3 A_2^3\right)\sin(\omega t + \varphi) \\ &+ \frac{a_2 A_2^2}{2}\cos(2\omega t + 2\varphi) - \frac{a_2 A_1^2}{2}\cos(2\omega t) \\ &- \frac{a_3 A_2^3}{4}\sin(3\omega t + 3\varphi) - \frac{a_3 A_1^3}{4}\sin(3\omega t)\,, \end{aligned} \tag{3.6}$$

where $A_1 = G_p A_0$ and $A_2 = G_n A_0$.

Equation (3.6) shows that an offset voltage and a second harmonic will be present at the output signal.

Figure 3.12 depicts a simulated output signal spectrum for an input signal of amplitude equal to 1 V and frequency of 1 kHz. Figure 3.12(a) shows the case when the output signals are balanced in amplitude and phase while figure 3.12(b) illustrates when the output signal has 1 dB of amplitude imbalance and $\varphi = 0.0873$ radian of phase imbalance.



(a) Ouptut signal spectrum for balance conditions (b) Ouptut signal spectrum for imbalance conditions

Figure 3.12: Simulated output signal spectra in balance and imbalance conditions for an input signal of 1 V amplitude and frequency of 1 kHz

3.2.2 Sources of Errors in the ADC

In Σ-Δ ADCs, the sources of errors mainly arise from the first integrator of the Σ-Δ modulator, apart from the topology and the architecture [4, 12, 18, 47].

The sources of errors can be divided into two categories: intrinsic noise and component non-idealities. Intrinsic noise is inherent to electronic devices, such as amplifiers $1/f$ noise and thermal noise. Component non-idealities include mismatches in capacitors and operational amplifiers gain errors [12, 47, 48].

As the Σ-Δ ADC is built with switched capacitors technique the integrator is affected by: i) finite open-loop gain, ii) mismatched capacitors and iii) limited bandwidth and slew rate. The first two groups produce distortion and deviations in the output signal of the ADC alike the input buffer and the FDA. Therefore, to estimate the influence of these errors on the performance of the ADC the same analysis performed when analysing the input buffer and the FDA can be applied in this case. In addition, finite open-loop gain increases the noise in the frequency band of interest.

The third group may be interpreted as a non-linear gain [49], therefore these errors produce harmonic distortion reducing the performance of the Σ-Δ modulator.

Moreover, a multi-bit topology has a multi-bit quantizer, therefore a multi-bit DAC is required in the feedback loop, as a consequence any non-linearity in the output signal of the DAC is directly added to the input signal to the modulator. As a consequence, special care in the design of the first modulator DAC in a multi-bit topology has to be taken into account [4, 47].

An analysis of the modulator is very complex to do analytically. Many authors have done the error and distortion analysis by behavioral modeling and simulation [12–14, 47–51]. Similar procedures are followed in this section by starting the analysis of component non-idealities, then the intrinsic noise is analyzed, following with the finite bandwidth and slew rate, and ending with the analysis of the Σ-Δ ADC input impedance.

3.2.2.1 Component Non-Idealities

In order to illustrate errors due to component non-idealities in the Σ-Δ ADC's first stage a numerical simulation was performed. This simulation was carried out using finite difference equations. The ideal integrators in the Σ-Δ ADC first stage were replaced by real integrators as shown in figure 3.13(a).

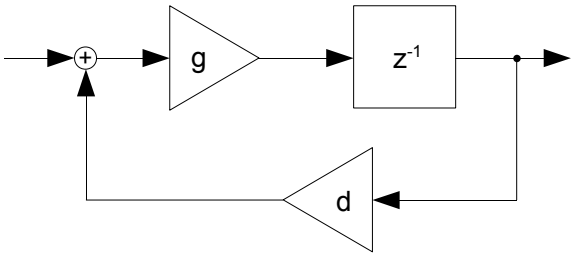
The transfer function of an ideal integrator is depicted in equation (3.7a) while equa-

tion (3.7b) shows the transfer function of a real integrator.

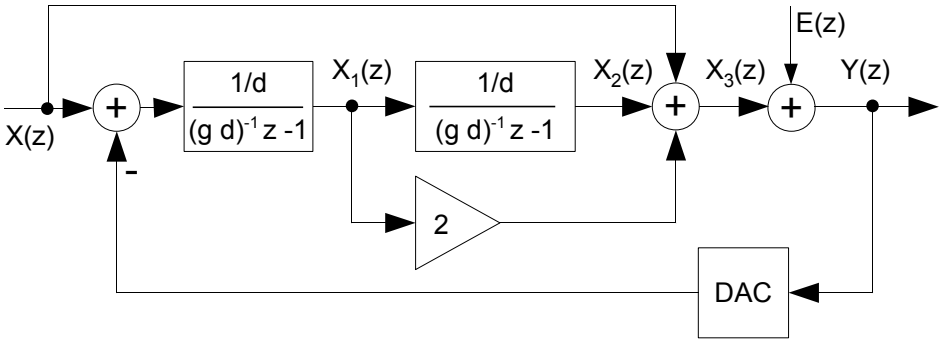
$$H_{ideal}(z) = \frac{1}{z-1} \tag{3.7a}$$

$$H_{real}(z) = \frac{1/d}{(gd)^{-1}z-1} \tag{3.7b}$$

Figure 3.13 shows the z-domain linear model for the real modulator used in the simulation.



(a) Block diagram for a real integrator



(b) Linear model for the ADC first modulator using real integrators

Figure 3.13: Z-domain linear model for the ADC first modulator using real integrators

The simulated input signal of the modulator was a sinusoidal waveform with an amplitude equal to 40 % of the ADC full scale with frequency of 1 kHz, to not overload the modulator. The sampling rate was 16384 kHz and the integrator gain factors were $g = d = 0.985$ and $g = d = 0.99999$ for the first and the second integrators, respectively, these values have been arbitrarily chosen close to 1 to emphasize gain deviation in real integrators.

Figure 3.14 compares the frequency spectra at the output of the real modulator, considering finite open-loop gain, and at the ideal modulator.

As expected, the real modulator increases noise at low frequencies and adds harmonic distortion. These noise and distortion may be fed to next stages in the ADC and may appear at the digital output.

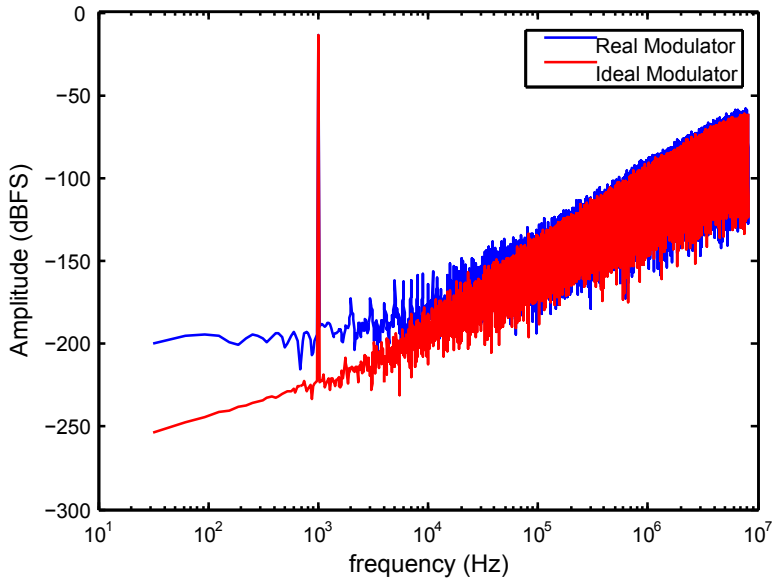


Figure 3.14: Simulated output spectra of the Σ-Δ ADC AD7763 first stage. In the case of a real integrator the noise in the low frequency range is higher than in the case of an ideal integrator

3.2.2.2 Intrinsic Noise

Intrinsic noise is generated internally in the device. Since the ADC is based on switched-capacitor technology, one source of noise is referred as switches thermal noise which is generated by the finite resistance of the switches. A second source of intrinsic noise is the amplifiers 1/f noise.

Intrinsic thermal noise has a white spectrum and a wide band limited by the time constant of the switched-capacitors or by the bandwidth of the device amplifiers. Modeling the input sampling switch as a series resistor with resistance R_{on} generating a thermal noise $v_n^2 = 4kTR_{on}\Delta f$, where k is the Boltzmann's constant, T is the absolute temperature and Δf the bandwidth. The noise $\bar{v_n^2}$ is sampled at the capacitor C_s at the sampling rate f_s as shown in figure 3.15

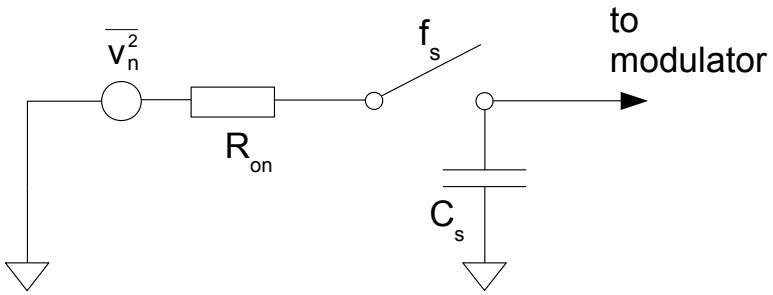


Figure 3.15: Simplified model of the input sampling capacitor

The total noise power e_T^2 can be estimated by evaluating the integral [47]

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_s)^2} df = \frac{kT}{C_s}\,. \tag{3.8}$$

Since the ADC has a bandwidth equal to $f_s/2$, the noise power is aliased to the band from 0 to $f_s/2$, the resulting noise spectrum is white with a spectral density

$$S(f) = \frac{2kT}{f_s C_s}\,. \tag{3.9}$$

As the ADC employs a double sampling technique [23] the thermal noise is sampled twice, so that the spectral density results in

$$S(f) = \frac{4kT}{f_s C_s}\,. \tag{3.10}$$

Intrinsic thermal noise will increase the noise floor of the ideal modulator. Thus, the noise level depicted in figure 3.14 is expected to increase.

3.2.2.3 Finite Bandwidth and Slew Rate

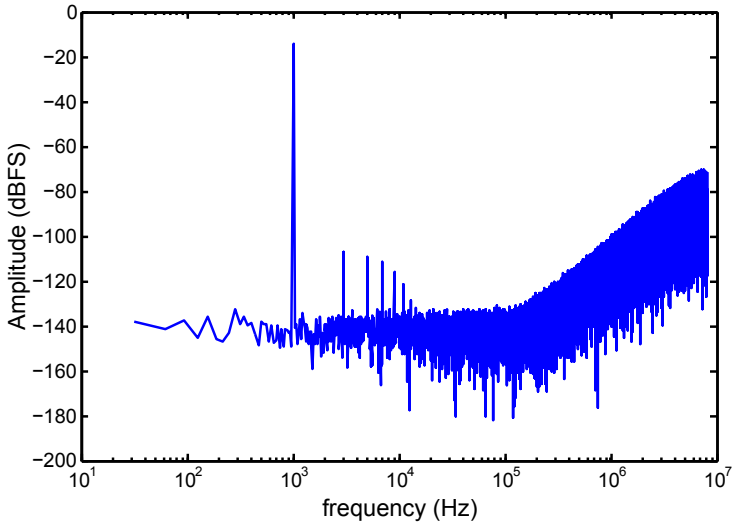
Finite bandwidth and slew rate will produce harmonic distortion [48–50]. To show these effects a simulation was performed assuming a sinusoidal input signal with frequency 1 kHz and amplitude 40 % of the ADC full scale. Because there is no information of the bandwidth and the slew rate of the ADC in the datasheet, these parameters were arbitrarily chosen. In order to point out the harmonic distortion two set of parameters were used. They are presented in table 3.1.

Table 3.1: Parameters used in the simulation of finite bandwidth and slew rate

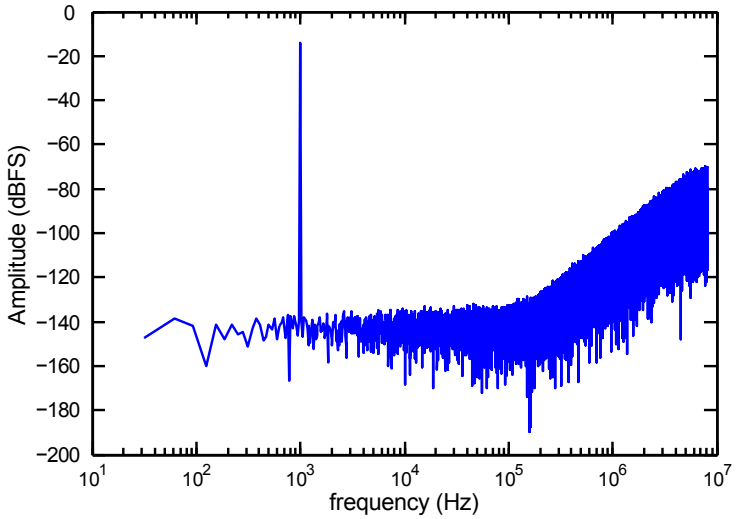
Σ-Δ Modulator Parameter	Values	
	Set 1	Set 2
Bandwidth (BW)	200 MHz	200 MHz
Slew rate (SR)	14.5 V/μs	150 V/μs
C_S	1 pF	1 pF

Figure 3.16 plots the simulated output spectrum of the modulator including thermal noise, finite bandwidth and slew rate. It is possible to observe that thermal noise increases the noise floor at low frequencies, while the slew rate in conjunction with the finite bandwidth produce harmonic distortion (figure 3.16(a)). Increasing the slew rate parameter from 14.5 V/μs to 150 V/μs (a value within the typical range of 100-300 V/μs

for some Σ-Δ modulators [12]) improves the harmonic distortion as can been seen in figure 3.16(b).



(a) BW=200 MHz, SR=14.5 V/μs



(b) BW=200 MHz, SR=150 V/μs

Figure 3.16: Simulated output signal spectrum of the AD7763 first modulator including thermal noise, finite bandwidth and slew rate

3.2.2.4 Input Impedance

Another source of error in the ADC is the finite input impedance. Based on the analysis performed in [47] and in the Σ-Δ ADC datasheet [27] the input stage can be modeled as in figure 3.17. C_{IN} represents the equivalent input capacitance, C_{SC} the equivalent sampling capacitors and R_{eq} and C_{eq}, the equivalent output impedance of the FDA (see figure 3.4). C_{IN} and C_{SC} in conjunction with R_{eq} and C_{eq} form a low-pass filter. Usually $C_{eq} \gg C_{SC}$,

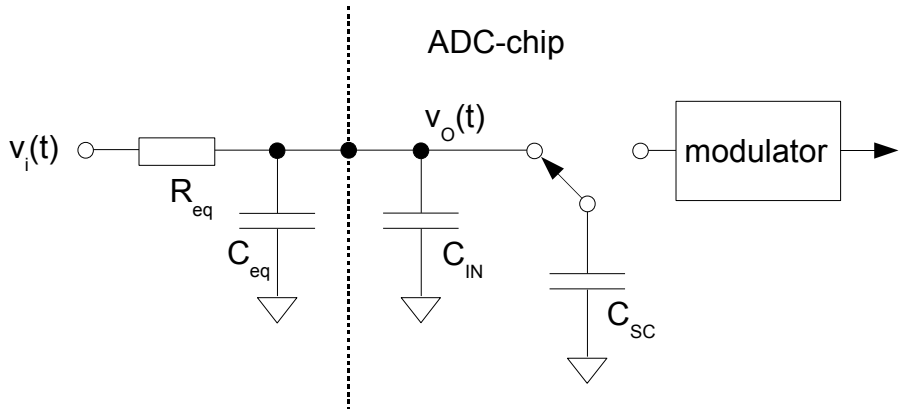


Figure 3.17: Equivalent model for the ADC input stage

thus C_{SC} can be considered as an equivalent resistor, at the sampling frequency f_s, of value $R_{C_{SC}} = 1/(f_s\, C_{SC})$ and will attenuate the input signal to a degree depending on the value of R_{eq}. This attenuation can be estimated by

$$v_o(t) = \frac{R_{C_{SC}}}{R_{C_{SC}} + R_{eq}}\, v_i(t)\,. \tag{3.11}$$

In addition, C_{IN} may exhibit voltage dependence. As it has been described in [52] voltage dependent capacitance can be modeled as

$$C(v) \approx C_0\, \left(1 + \alpha_1 v + \alpha_2 v^2\right)\,, \tag{3.12}$$

where α_i are the coefficients of Taylor series expansion of $C(v)$. This voltage dependence will produce harmonic distortion which, indeed, will degrade the signal-to-noise ratio of the ADC as has been shown in [13, 51].

3.2.3 Sources of Error in the Voltage Reference

The performance of the voltage reference limits the performance that the ADC can reach. Indeed, the ADC will follow any deviation of its voltage reference. The output of an ideal ADC with a mid-thread quantizer (see figure 2.5), provided that the quantizer is not overloaded, is [53]

$$Q\left[v_i(t)\right] = \left\lfloor v_i(t)\frac{2^N}{FSR} + \frac{1}{2}\right\rfloor \tag{3.13}$$

where $v_i(t)$ is the input voltage to the ADC and FSR is the ADC full-scale range, commonly the voltage reference value $FSR = V_{REF}$. The $\lfloor\cdot\rfloor$ is the greatest integer

function or integer value [54]. Then, equation (3.13) becomes,

$$Q\left[v_i(t)\right] = \left\lfloor v_i(t)\frac{2^N}{V_{REF}} + \frac{1}{2}\right\rfloor \tag{3.14}$$

Equation (3.14) shows that the ADC output is inversely proportional to its voltage reference. As a result, any deviation in the voltage reference value due to linear drift, loading effects, etc. is translated to the output digital code.

3.2.3.1 Loading Effects

The designers of the Σ-Δ AD7763 ADC had reported that the front-end modulator draws a nonlinear current from the voltage reference source [23]. This nonlinear current has a quadratic dependence with the input signal amplitude as described by [55]

$$I_{REF} \propto \frac{V_{REF}}{2} f_s\, C_T \left(1 - \frac{v_i^2}{V_{REF}^2}\right) \tag{3.15}$$

where C_T is the equivalent input capacitance of the ADC front-end, f_s is the sampling rate, V_{REF} is the voltage reference value, v_i is the input signal amplitude. If this current is drawn through a finite voltage reference source output resistance R_s, a nonlinear modulation of the voltage reference voltage is seen by the front-end modulator as [55]

$$V_{REF_M} \approx V_{REF}\left[1 + \left(\frac{v_i}{V_{REF}}\right)^2 (R_s\, f_s\, C_T)\right]. \tag{3.16}$$

This modulation on the voltage reference introduce harmonic distortion which depends on the ratio between R_s and $f_s\, C_T$ as indicated in reference [55]. To minimize the harmonic distortion R_s has to be as low as possible (0.04 Ω for a 100 dB 3-rd harmonic), therefore the designers of the Σ-Δ ADC have added a wide bandwidth buffer to reduce the output resistance R_s of the voltage reference source [23].

The current drawn by the ADC from the voltage reference circuit has been measured at different sampling rates with the input of the system shorted ($v_i = 0\,\text{V}$). For this propose the voltage drop in a 10 Ω resistor connected in series between the voltage reference buffer output and the ADC voltage reference input pin has been measured using a high resolution and high accuracy digital voltmeter (DVM) Agilent 3458A in DC voltage mode (DCV), 10 V range and NPLC=50. Results are shown in table 3.2. These results show a linear dependence of the current drawn by the ADC as it is described by equation (3.15) when ($v_i = 0$ V).

Also, the dependence of the voltage reference value with the ADC sampling rate

Table 3.2: Voltage reference input current I_{REF}

Equivalent Sampling rate (kHz)	I_{REF} (μA)
64	34.0
32	16.9
16	8.3
8	4.0
4	2.0

was measured during three days, with the system input shorted ($V_i = 0\,\text{V}$), using a high resolution and high accuracy digital voltmeter (DVM) Agilent 3458A in DCV mode, 10 V range and NPLC=50. Figure 3.18 shows the results. They are summarized in table 3.3.

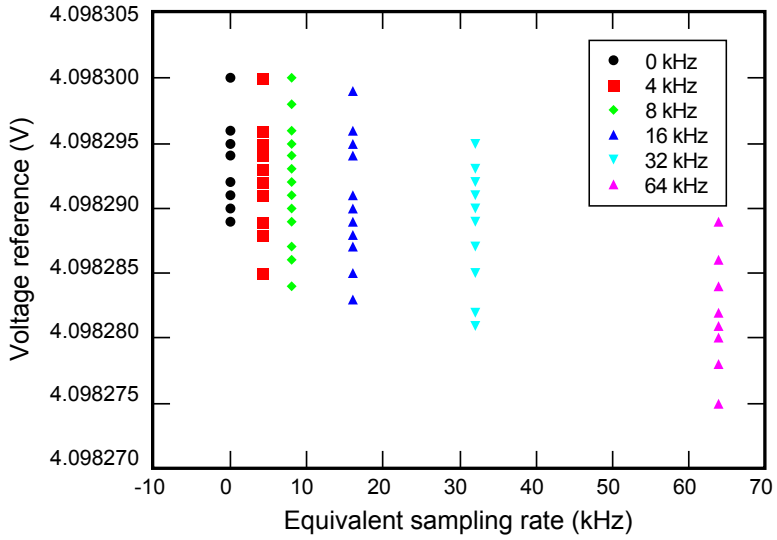


Figure 3.18: Voltage reference value vs Equivalent sampling rate

From these results it is clear to see a dependence of the voltage reference value with the ADC sampling rate. The changes in V_{REF} are bounded by ± 7.5 μV in the worst case. Therefore, with this limit the uncertainty contribution to the output signal of the ADC may be estimated to be equal to $\pm\,1.2\,\mu\text{V/V}$, assuming a rectangular probability distribution [56].

3.2.4 Sources of Error from the Sampling Clock

The main source of error in the sampling clock module is the time jitter. For the AD9852 device a peak-to-peak time jitter (t_{jp-p}) has been measured to be $\leq$ 400 ps [41]. The time jitter has an impact on the SNR, as a consequence, the ENOB is reduced as the

Table 3.3: Measured voltage at the reference input pin of the ADC. The Type A uncertainty of the measured values is equal to 0.4 μV/V

Equivalent sampling rate (kHz)	Maximum (V)	Minimum (V)	Semi-interval (μV)	Mean (V)	s (μV)
0	4.098300	4.098289	5.30	4.098294	3.05
4	4.098300	4.098285	7.55	4.098293	4.22
8	4.098300	4.098284	7.90	4.098292	4.50
16	4.098299	4.098283	7.75	4.098291	4.39
32	4.098295	4.098281	7.15	4.098288	4.17
64	4.098289	4.098275	7.00	4.098282	3.83

time jitter increases.

The effect of the time jitter in the SNR can be predicted replacing σ_e with σ_j in equation (2.11), hence the SNR becomes

$$SNR = 10\,\log\left(\frac{\sigma_s^2}{\sigma_j^2}\right), \tag{3.17}$$

where σ_s^2 is the power of the input signal and σ_j^2 is the variance (or power) of the amplitude error caused by sampling clock time jitter. Assuming a sinusoidal input signal as

$$v_i(t) = A_0\,\sin(\omega_0\,t) \tag{3.18}$$

The derivative of $v_i(t)$ with respect to t is

$$\frac{\partial v_i(t)}{\partial t} = A_0\,\omega_0\,\cos(\omega_0\,t). \tag{3.19}$$

The derivative is maximum when $\cos(\omega_0\,t) = 1$, i.e. $t = 0$, hence the rms value is

$$\frac{\partial v_i(t)}{\partial t}\Big|_{rms} = \frac{A_0}{\sqrt{2}}\,\omega_0\,. \tag{3.20}$$

Renaming the infinitesimal $\partial v_i(t)$ as σ_j, the infinitesimal ∂t as Δt and rewriting equation (3.20)

$$\frac{\partial v_i(t)}{\partial t}\Big|_{rms} = \frac{\sigma_j}{\Delta t} = \frac{A_0}{\sqrt{2}}\,\omega_0\,, \tag{3.21}$$

it is possible to estimate the rms amplitude error σ_j due to an rms time jitter Δt as [57, 58]

$$\sigma_j = \frac{A_0}{\sqrt{2}}\,\omega_0\,\Delta t. \tag{3.22}$$

Then, the degradation in the SNR by the time jitter is

$$\begin{aligned} SNR &= 10\,\log\left(\frac{\sigma_s}{\sigma_j}\right)^2 = 10\,\log\left(\frac{A_0/\sqrt{2}}{A_0/\sqrt{2}\,\omega_0\,\Delta t}\right)^2 \\ &= 10\,\log\left(\frac{1}{\omega_0\,\Delta t}\right)^2. \end{aligned} \tag{3.23}$$

The theoretical SNR for an oversampling Σ-Δ ADC is given by [18]

$$SNR = 20\log\left(\frac{\sigma_s}{\sigma_e}\right) + 10\log\left(OSR\right) = 20\log\left(\frac{\sigma_s}{\sigma_e}\sqrt{OSR}\right). \tag{3.24}$$

Assuming as only contribution to the total noise the time jitter σ_j, equation (3.23) becomes

$$SNR = 20\,\log\left(\frac{\sqrt{OSR}}{\omega_0\,\Delta t}\right). \tag{3.25}$$

For instance, if the frequency of the input signal is 2 kHz and the peak-to-peak time jitter for this module is 400 ps, which corresponds to an rms time jitter of 66.67 ps. Then, the SNR for an ideal Σ-Δ ADC with an OSR = 256 is

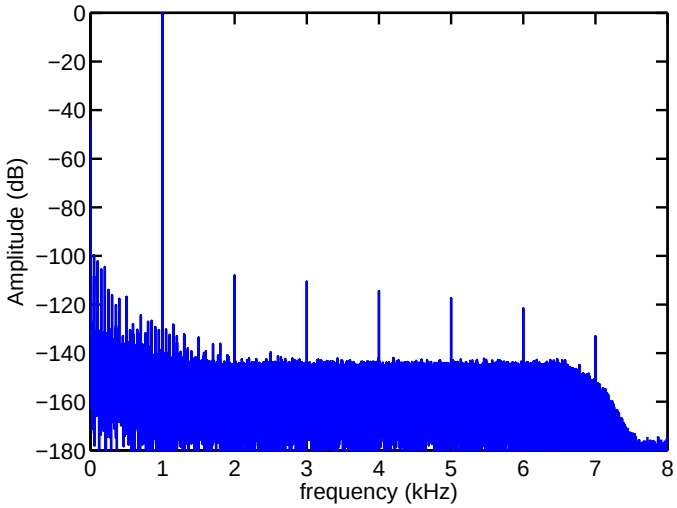
$$SNR = 20\,\log\left(\frac{\sqrt{256}}{2\,\pi\,2000\,\mathrm{Hz}\,66.67\,\mathrm{ps}}\right) = 145.61\,\mathrm{dB}.$$

Computing the ENOB using equation (2.14) results in 23.89-bits, that is a reduction in resolution of 0.11 bit. As a conclusion, the effect of clock time jitter in this system is negligible.

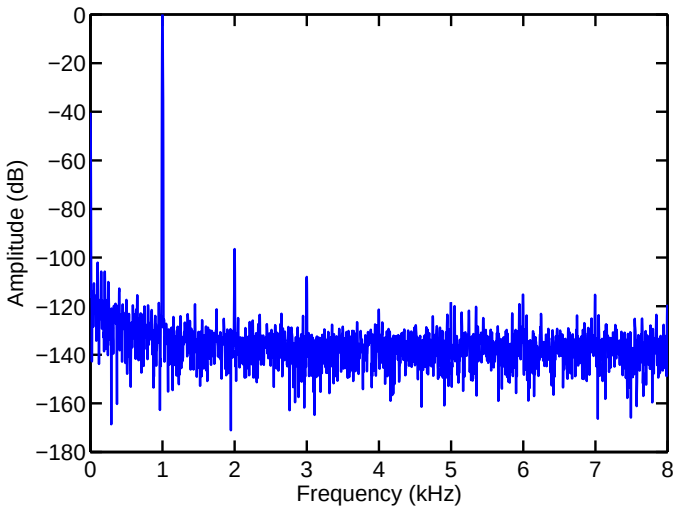
3.3 Example of a Measured Signal

To illustrate the imperfections of the system a test was performed. A low distortion sinusoidal signal with a peak amplitude of 1 V and frequency of 1 kHz was applied to the system using a low distortion source, the Stanford Research System model DS360 [59], which has a total harmonic distortion better than -110 dB in the frequency range from 0.01 Hz to 5 kHz at output amplitudes of 1 V_{rms}. This signal was sampled at an equivalent sampling of 16 kHz with a decimation rate of 256. Figure 3.19 depicts the computed frequency spectrum of the measured signal in which harmonic distortion, DC offset, noise and spurious frequency components are appreciated. In conjunction, the same signal was measured using a commercial device with a typical total harmonic distortion of -106 dBc at 100 kHz input signal frequency, the PXI-5922 system from

National Instrument Corporation [60] in order to compare the measured signal spectra as shown in figure 3.19(b).



(a) Σ-Δ sampling system output spectrum



(b) NI PXI-5922 output spectrum

Figure 3.19: Measured signal spectrum. In this figure is visible the harmonic distortion, in-band noise and DC offset.

As can be seen from figure 3.19 the amplitude of the harmonics (from the 3^{rd} harmonic up to the 6^{th} harmonic) present on the sampled signal by both devices are comparable and it is unclear to conclude whether the distortion harmonic is produced by the instruments or by the source. The PXI-5922 has higher noise floor than the Σ-Δ sampling system. However, the Σ-Δ sampling system shows the 3^{rd} and the 4^{th} harmonic levels slightly higher than 110 dB (above the specification of the source). Hence, the Σ-Δ sampling system may be compensated for these deviations to reach the required performance in metrology applications.

Chapter 4

Models for Analog-to-Digital Converters

Metrology applications demand high accuracy in the determination of the measurand. A practical ADC cannot provide the needed performance due to imperfections such as gain deviation, thermal drift, non-linearity, etc. As a consequence, the ADC readouts may have deviations from the original signal applied to its input. In general, the ADC imperfections can be corrected and/or post-compensated by modeling the ADC in order to reconstruct the input signal with high accuracy. This chapter introduces models and methods which are commonly used to describe ADCs. In particular the Hammerstein model and the method employed to determine the model parameters are described.

4.1 Modeling

Analog-to-Digital converters modeling for pre- and post- correction have been studied for many years; for a survey on ADC modeling and compensation see references [10, 11]. As a result, different methods have been investigated which can be classified as follows:

1. look-up table methods,
2. dithering methods,
3. methods based on model inversion and
4. architecture-based methods.

A description of these methods can be found in reference [11] and in the citations within.

In this thesis, the model inversion method is employed to post-compensate the sampling system for deviations and non-linearities in order to achieve an accuracy of 5 parts

in 10^6 of the measured value. Although this model is applied to a Σ-Δ ADC, its usage can be extended to other types of ADCs or systems.

In Figure 4.1 the sampling system is represented by the transfer function $g_D(\cdot)$. If a continuous time sinusoidal signal $x(t) = A_o \sin(2\pi f_o t)$ is applied to the system with a non-linear transfer function $g_D(\cdot)$, this non-linear function will introduce distortions in the input signal producing a discrete time signal $y[n]$.

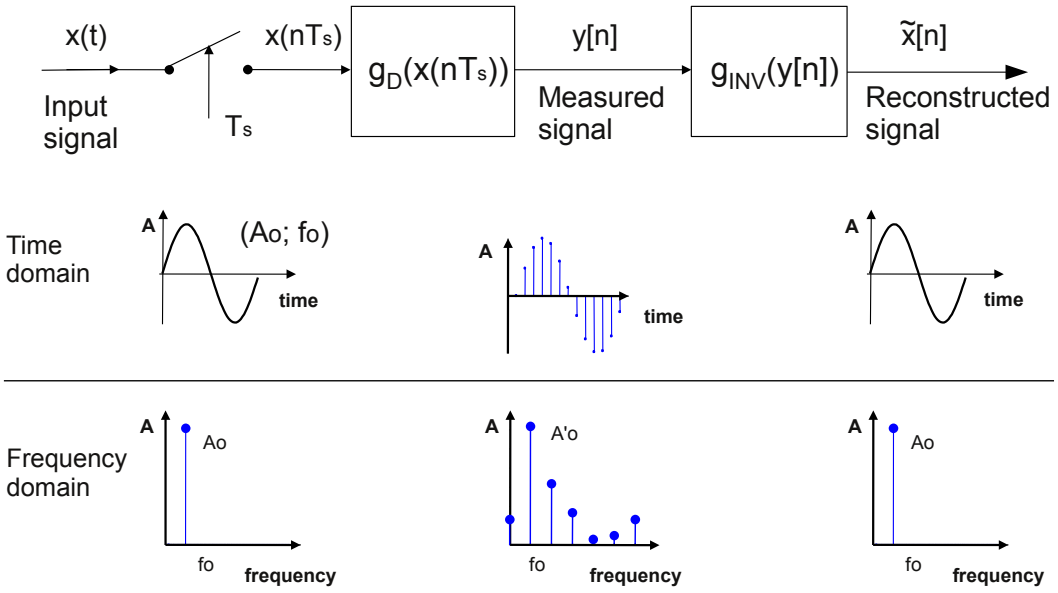


Figure 4.1: Modeling process

The distortion and imperfections in the measured signal $y[n]$ must be removed in order to reconstruct the input signal. This can be done by finding a model with a transfer function $g_R(\cdot)$ which compensates for the non-linearities and deviations of $g_D(\cdot)$. A straightforward solution is to find $g_R(\cdot)$ as the inverse of $g_D(\cdot)$.

4.2 Non-linear Models

The non-linear models used in this thesis are introduced in this section. A complete coverage of this topic can be found in reference [15].

4.2.1 Power Series Expansion

A power series in variable x is the infinite sum

$$s(x) = \sum_{i=0}^{\infty} a_i x^i \tag{4.1}$$

where a_i are integers, real numbers, complex numbers, or any other quantities of a given type. An example of a power series is a polynomial in variable x of order N as

$$p(x) = \sum_{k=0}^{N} c_k x^k \tag{4.2}$$

where c_k are the coefficients of the polynomial $p(x)$.

A simple representation of a non-linear system is to use polynomials of any degree, based on the Weierstrass theorem [61], which states that

> *Any continuous function defined on an interval [a,b] can be uniformly approximated as closely as desired by a polynomial function.*

The output $y[n]$ of the non-linear system $g_D(\cdot)$, illustrated in figure 4.2, can be expressed as

$$y[n] = g_D(x[n]) = a_0 + a_1 x[n] + a_2 x^2[n] + \cdots + a_N x^N[n]\,. \tag{4.3}$$

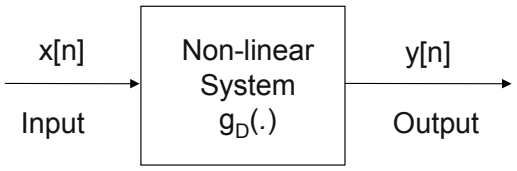


Figure 4.2: Non-linear system block diagram representation

In order to compensate the system $g_D(\cdot)$ for non-linearities a system $g_R(\cdot)$, if exists, has to be found by inverting the transfer function $g_D(\cdot)$.

The process of compensation using power series expansion is illustrated in figure 4.3, where the non-linearities introduced by the system $g_D(\cdot)$ on the input $x[n]$ are compen-

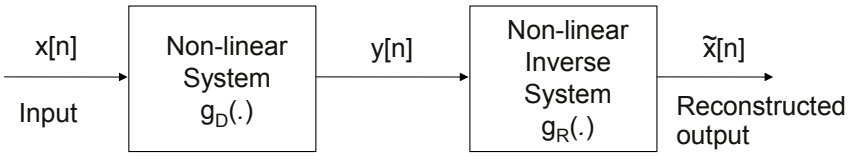


Figure 4.3: Non-linearities compensation by power series expansion modeling

sated by the non-linear system $g_R(\cdot)$. Hence, the reconstructed output $\tilde{x}[n]$ is calculated and reconstructed the original input $x[n]$ as equation (4.4) shows.

$$\tilde{x}[n] = g_R(y[n]) = g_R(g_D(x[n])) \approx x[n]. \tag{4.4}$$

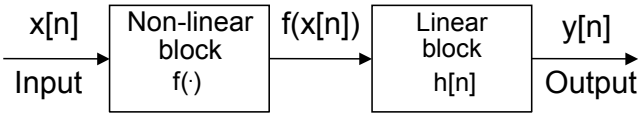
Although all terms up to the order of the system $g_R(\cdot)$ are canceled, the coefficient cross-products add higher order terms to the reconstructed output [62, 63]. The values

of the coefficients depend on the signal amplitude used to obtain the parameters of the model, thus it is important to use amplitudes close to the system full scale. If this is the case, the effects of these high order terms on the output are negligible. However, when using this compensation technique the influence of these high order terms must be evaluated.

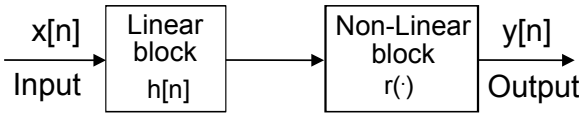
4.2.2 Block-Oriented Models

A block-oriented model consists of an interconnection of two or more blocks. The interconnection can be parallel, series or a combination of both and may include feedback branches. Each block represents a different part of the system to be modeled. When the systems to model exhibits static non-linearities and linear dynamics three different block oriented models are usually employed [15]:

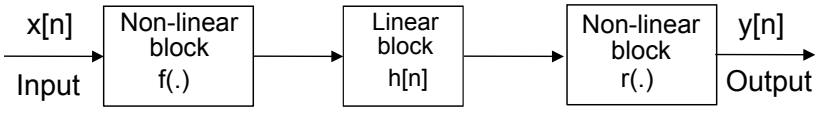
- *Hammerstein model*: a block oriented model with static non-linearity at the input (figure 4.4(a)).
- *Wiener model*: a block oriented model with static non-linearity at the output (figure 4.4(b)).
- *Hammerstein-Wiener model*: a combination of both type of models (figure 4.4(c)).



(a) Hammerstein block oriented model



(b) Wiener block oriented model



(c) Hammerstein-Wiener block oriented model

Figure 4.4: Block oriented models

The static non-linear block of these models can be any non-linear operator, e.g. power series or piece-wise defined function.

If the linear block of the Hammerstein model has an impulse response $h[n]$ then the output $y[n]$ will be

$$y[n] = f(x[n]) * h[n], \tag{4.5}$$

where $*$ denotes the convolution sum [17].

4.3 Model for the System

This section describes the model for the designed sampling system.

4.3.1 System Block Diagram

A simplified block diagram for the sampling system is depicted in figure 4.5. In the

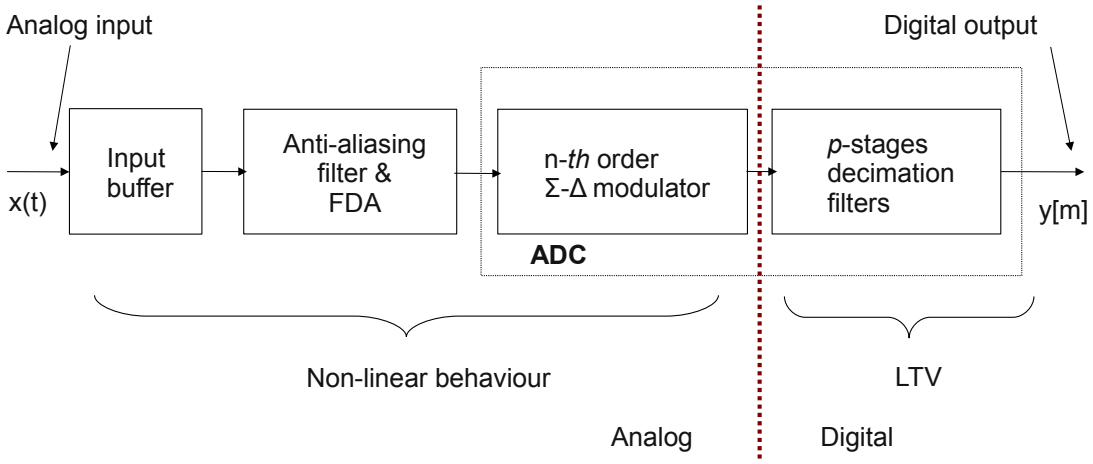


Figure 4.5: Simplified block diagram of the sampling system

diagram the analog part can be distinguished from the digital part. The analog part consists of the input buffer, the fully differential amplifier and the n-*th* order modulator of the Σ-Δ ADC. The digital part includes the p-stages decimation filters.

The analog part includes electronic components, therefore it is likely to have a non-linear behavior as has been introduced in section 3.2. The digital part is a linear time varying system LTV [64, 65], consequently, the whole system has a static non-linearity at its input and a linear transfer function at its output. Thus, a suitable post-compensation model is one which can represent input static non-linearities followed by a linear transfer function: the Hammerstein model.

The Hammerstein model, with some modifications, has been applied by other authors to post-compensate ADCs [66, 67]. In [66] the model was used to compensate a self-designed 4-bit flash and a 7-bit pipeline ADC. The non-linearities were modeled using polynomials while for the linear block the authors applied a finite impulse response (FIR) filter. In [67], the non-linear block was represented by a piece-wise function while the linear block was extended to a parallel configuration in order to have a set of filters with

different cut-off frequencies. With this approach they compensate a commercial 12-bit pipeline ADC.

In this thesis, the Hammerstein model is applied to post-compensate a 24-bit Σ-Δ ADC including the analog electronics.

4.3.2 The Hammerstein Model

The Hammerstein model is depicted in figure 4.6. As has been introduced in section 4.2.2 the Hammerstein model has two blocks: the input block, which is a static non-linear operator and the output block that is a linear system.

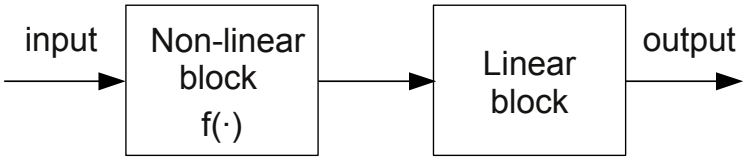


Figure 4.6: The Hammerstein model block diagram

4.3.2.1 Non-linear Block

The non-linear block is parametrized in terms of a power series expansion, see section 4.2.1. As was presented in section 3.3 the system is expected to have non-linear behavior. Thus, this non-linear behavior will be compensated by a 4^{th}-order polynomial. As has been illustrated in section 3.3 the system introduces harmonic distortion to the sampled signal. The amplitude level of higher harmonics order than fourth are below 120 dB, therefore the deviation that they may introduce to the sampling signal can be neglected to achieve high accuracy and performance when measuring alternating signal.

4.3.2.2 Linear Block

The quantized data of the ADC are decimated by 3-stage digital filters. The overall frequency response of these filters attenuates the measured signal. To compensate the amplitude deviations the inverse frequency response has to be found and then applied to the measured signal for correction. In this block, the inverse frequency response of the ADC's FIR filters is implemented.

4.3.3 The Complete Model for the System

The complete model for the sampling system is depicted in figure 4.7. The first block represents the non-linear transfer function of the sampling system connected in cascade to

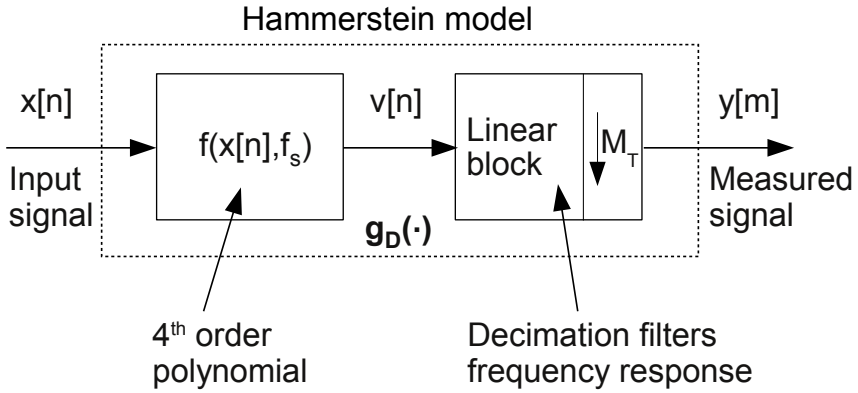


Figure 4.7: Complete Hammerstein model for the sampling system

a second block which in turn represents the linear transfer function of the ADC decimation filters. These blocks complete the Hammerstein model with an overall transfer function $g_D(\cdot)$. Then follows to find an inverse function $g_R(\cdot)$ such that

$$g_R\left(g_D(\cdot)\right) \approx 1\,. \tag{4.6}$$

Then, the input signal $x[n]$ can be reconstructed to a M_T-downsampled [68] signal $\tilde{x}_D[m]$ from the measured signal $y[m]$ by the following expression

$$\tilde{x}_D[m] = g_R\left(g_D(y[m])\right) \approx x_D[m]\,. \tag{4.7}$$

To obtain the input signal $\tilde{x}[n] \approx x[n]$ any interpolation procedure can be use, such as, zero-order or linear interpolation as described in [69], resulting $\tilde{x}[n] = \tilde{x}_D[m/L_T]$ (with $L_T = M_T$ in this case). In this thesis a zero-order interpolation will be use as it will be indicated in section 6.7.1.

Since the non-linearities depend on the sampling rate f_s, as it has been stated in section 3.2.2, the model has to be extend to different sampling rates. As a consequence, each sampling rate has a different non-linear function $f(\cdot, f_s)$.

4.4 Parameter Identification

The Hammerstein model has been investigated by many authors and different methods to identify the model parameters have been studied and developed, see reference [70]. The internal structure of the Hammerstein model (see figure 4.8) indicates that it is useful to separate the non-linear block from the linear block in order to identify the parameters.

Therefore, the identification is carried out by two techniques as follows:

1. The non-linearities are identified in the time domain by a power series expansion

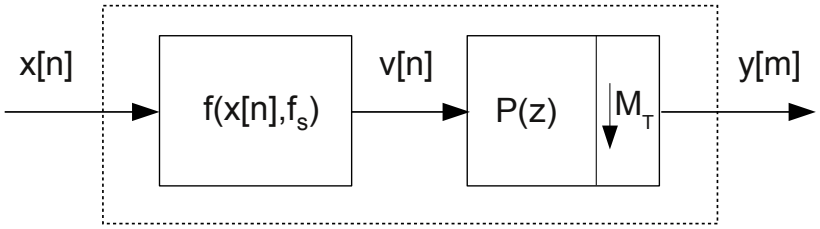


Figure 4.8: Simplified diagram of the Hammerstein model, where f(x[n],f_s) represents the non-linear block while P(z) represents the linear block.

approach.

2. The linear block is identified using a frequency domain method.

4.4.1 Identification of the Non-linear Block

The non-linear block consists of a fourth order polynomial, since higher order non-linearities do not contribute significantly, as

$$f(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4. \tag{4.8}$$

In order to identify the coefficients of the polynomial a_i $(i = 1, \ldots, 4)$ a well known, noiseless and no-drift signal has to be applied to the system.

Thus, from the measured output signal of the ADC and the well-known input signal, the coefficients a_i of the transfer function are calculated fitting the input-output data set by regression analysis using the least-squares method for polynomials [71, 72].

The output $v[n]$ of the non-linear block is

$$f(x[n]) = v[n] = a_0 + a_1 x[n] + a_2 x^2[n] + a_3 x^3[n] + a_4 x^4[n], \tag{4.9}$$

with $n = 1, 2, \ldots, N$. In matrix notation equation (4.9) becomes

$$\mathbf{v} = \mathbf{X}\,\theta, \tag{4.10}$$

where

$$\mathbf{v} = (\, v[1]\, v[2]\, \ldots\, v[N]\,)^T, \tag{4.11}$$

is the vector of ADC readouts.

$$\mathbf{X} = \begin{pmatrix} 1 & x[1] & x^2[1] & x^3[1] & x^4[1] \\ 1 & x[2] & x^2[2] & x^3[2] & x^4[2] \\ & & \vdots & & \\ 1 & x[N] & x^2[N] & x^3[N] & x^4[N] \end{pmatrix} \tag{4.12}$$

is the Vandermonde matrix of the input waveform and

$$\theta = (\, a_o\, a_1\, a_2\, a_3\, a_4\,)^T\,, \tag{4.13}$$

is the vector of coefficients (superscript T indicates transposition).

Hence, the vector θ can be found solving the set of linear equations (4.10) by means of the least-square method as

$$\begin{aligned} \mathbf{X}^T\mathbf{v} &= \mathbf{X}^T\mathbf{X}\,\theta \\ (\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T\mathbf{v} &= (\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T\mathbf{X}\,\theta \\ (\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T\mathbf{v} &= \mathbf{I}\,\theta. \end{aligned} \tag{4.14}$$

where $\mathbf{I}$ is the identity matrix.

Then it follows that, the forth order polynomial of equation (4.9) is inverted in order to obtain the polynomial $r(v[n])$ as

$$x[n] \approx \tilde{x}[n] = r(v[n]) = b_0 + b_1 v[n] + b_2 v^2[n] + b_3 v^3[n] + b_4 v^4[n]\,, \tag{4.15}$$

so that,

$$r(v[n]) = r\,(f(x[n], f_s)) = \mathbf{1} + \epsilon\,, \tag{4.16}$$

where ϵ represents any deviation or uncertainty due to the inversion process.

4.4.2 Identification of the Linear Block

The linear block with a transfer function $P(z)$ depicted in figure 4.8 is a three stage decimation filter. These stages are illustrated in figure 4.9

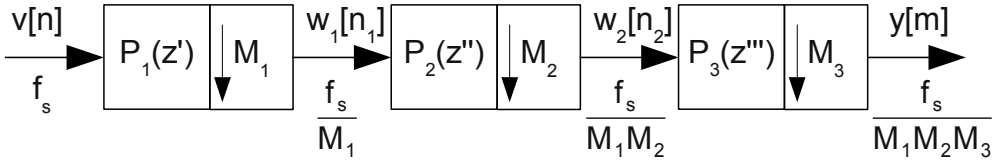


Figure 4.9: Block diagram of the ADC decimation filters stage

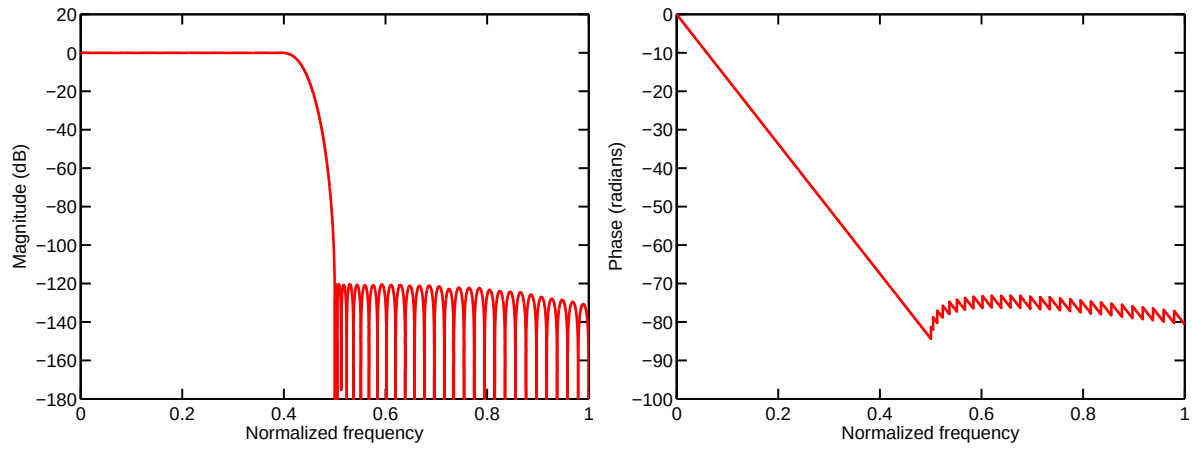
The sampling frequency of the input signal $v[n]$ is f_s, and the output sampling frequency or equivalent sampling frequency of the output signal $y[m]$ is f_s/M_T, where M_T is given by

$$M_T = M_1 \cdot M_2 \cdot M_3 \,. \tag{4.17}$$

The overall transfer function $P(z)$ of the decimation filters related to the equivalent sampling frequency f_s/M_T is given by

$$P(z) = P_1(z') \cdot P_2(z'') \cdot P_3(z''') \,, \tag{4.18}$$

where $P_i(z)$ is the transfer function of stage i. Replacing $z' = e^{j\,2\,\pi\,f M_1/f_s}$, $z'' = e^{j\,2\,\pi\,f M_1 M_2/f_s}$ and $z''' = e^{j\,2\,\pi\,f M_1 M_2 M_3/f_s}$, the overall frequency response can be obtained. The magnitude ($|P(e^{j\,2\,\pi\,f M_T/f_s})|$) and phase $\angle(P(e^{j\,2\,\pi\,f M_T/f_s}))$ are depicted in figure 4.10 for the whole frequency range in order to show the attenuation at frequencies above the Nyquist's frequency ($f = f_s/M_T/2$), resulting in an amplitude attenuation higher than 120 dB.



(a) Magnitude $|P(e^{j\,2\,\pi\,f M_T/f_s})|$

(b) Phase $\angle(P(e^{j\,2\,\pi\,f M_T/f_s}))$

Figure 4.10: Magnitude and phase of the overall decimation filters frequency response, normalized to the output sampling rate f_s/M_T

As can be seen from figure 4.10(b), the decimation filters are linear phase, therefore the frequency response is given by

$$P(e^{j2\,\pi\,f M_T/f_s}) = |P(e^{j2\,\pi\,f M_T/f_s})|\, e^{-j\,2\,\pi\,f M_T/f_s\,\alpha} \,, \tag{4.19}$$

which corresponds to a frequency response of a linear system with linear phase [69].

The compensation for the frequency response of these filters is the inverse of the overall frequency response $P(z)$. Because these filters have linear phase, no phase distortion is introduced by the filters, only a time delay which is determined by α. Thus, no correction

for phase is needed to be performed. The compensation for the magnitude of the frequency response is described in section 6.3.

4.5 Evaluation of the Uncertainty in the Model

4.5.1 Uncertainty Evaluation of the Non-linear Block

The type-A uncertainty evaluation is carried out as follows: first, the Allan deviation is computed on the measured data in order to obtain the observation time τ in which the system reaches the lower uncertainty. Second, the discrete time series is split according to this observation time. Finally, the type-A uncertainty is estimated on the model parameters and the combined uncertainty u_c is calculated.

4.5.1.1 Allan Deviation

To evaluate the model parameters uncertainty the Allan deviation [73] is computed on the measured discrete time series. The Allan deviation is the square root of the Allan variance of $y[n]$ and is given by

$$\sigma_y(\tau) = \sqrt{\sigma_y^2(\tau)}, \tag{4.20}$$

where the Allan variance $\sigma_y^2(\tau)$ is defined as [73]

$$\sigma_y^2(\tau) = \frac{1}{2}\left\langle (\bar{y}_{i+1}(\tau) - \bar{y}_i(\tau))^2 \right\rangle, \tag{4.21}$$

which can be calculated from [74]

$$\sigma_y^2(\tau) = \frac{1}{2(M-1)} \sum_{i=1}^{M-1} \left(\bar{y}_{i+1}(\tau) - \bar{y}_i(\tau)\right)^2, \tag{4.22}$$

where $\tilde{y}_i$ is the mean value of the i-th group of M successive measured values $y[n]$ over an observation time τ.

The Allan deviation is a powerful tool to characterize data series in the time domain. It can reveal typical noise processes which appear in measurements [75]. A typical Allan deviation plot for DC voltage measurements is illustrated in figure 4.11 in which three noise processes are observed: i) white noise (from 0 to τ_1), ii) $1/f$ or flicker noise (from τ_1 to τ_2) and iii) linear drift.

The Allan deviation plot depicted in figure 4.11 indicates which is the observation time τ to reach the lower type-A uncertainty σ_1 on this measurement process. Under

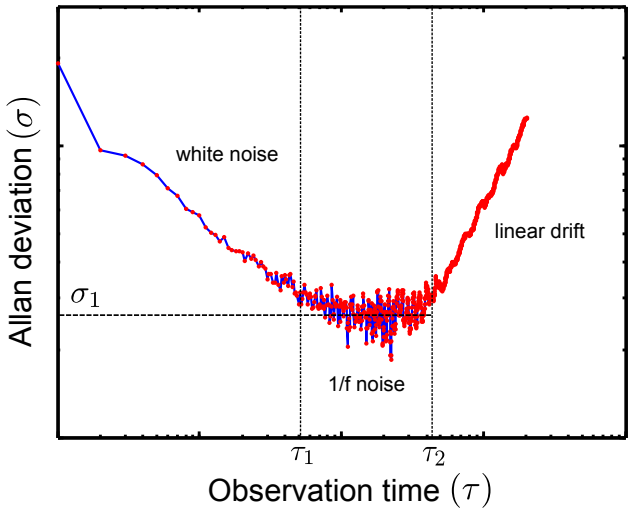


Figure 4.11: Typical Allan deviation for a DC voltage measurement

these conditions, the time series is considered as a white noise process with Gaussian distribution and the type-A uncertainty is directly the Allan deviation σ_1.

The observation time τ in which the time series can be divided was determined with the Allan deviation. Then, the method described in section 4.4.1 is followed to determine the parameters of the non-linear block of the model.

4.5.1.2 Type-A Uncertainty Estimation

To estimate the type-A uncertainty on each coefficient of the polynomial the variance-covariance matrix [71] of the input $x[n]$ and the output $v[n] = f(x[n], f_s)$ of the non-linear block of the system (see figure 4.8) is computed as follows

$$\mathbf{COV}\,(x, v) = s^2 \left(\mathbf{X}^T\mathbf{X}\right)^{-1}, \tag{4.23}$$

where s^2 is an estimator of the variance of the residuals $e_i = v[i] - \tilde{v}[i]$ of the adjustment and is given by

$$s^2 = \frac{\sum_{i=1}^{N} e_i^2}{df}, \tag{4.24}$$

where $df = N - P$ is the degrees of freedom (P is the number of coefficients, 5 in this case). Resulting the type-A uncertainty of each coefficient to be

$$u(a_i) = \sqrt{\text{diag}(\mathbf{COV}(x, v))}. \tag{4.25}$$

An estimation of the standard error of the fit adjustment is $\sqrt{s^2}$. This is an indication of the goodness of the fitting process and also estimates the maximum non-linearity deviation of the system.

When using the polynomial $r(v[n])$ to approximate the input $x[n]$ a complete set of new values are predicted, say $x_0[n]$ with $n = 1, 2, \ldots, N$ are fitted. To estimate the type-A uncertainty due to the polynomial fitting, the prediction interval $\tilde{\sigma_p}$ is computed for the fitted values $x_0[n] = r(v[n])$. The prediction interval can be obtained, as it is explained in reference [76], using the following equation

$$\tilde{\sigma_p} = s\,\sqrt{1 + \sigma_{x_0}}, \tag{4.26}$$

where σ_{x_0} is given by

$$\sigma_{x_0} = x_0 \left(\mathbf{X}^T\mathbf{X}\right)^{-1} x_0^T \tag{4.27}$$

Finally, the maximum of $\tilde{\sigma_p}$ is taken as an estimator of the uncertainty of the predicted values, thus

$$u_{x_0} = \max\left\{\tilde{\sigma_p}\right\}. \tag{4.28}$$

Chapter 5

Sigma-Delta Data Converter Characterization

The characterization process presented here involves the determination of metrics in order to obtain the performance of the ADC. The characterization is carried out in two regimes, dynamic and static. This chapter introduces these metrics and summarizes the performance results of the Σ-Δ ADC used in this thesis. The signal sources to evaluate the performance metrics of the ADC were: a pulse-driven Josephson waveform synthesizer to determine the metrics in dynamic regime and a binary Josephson waveform synthesizer for the static regime metrics. These two voltage standards are powerful tools to characterize ADCs when used in electrical metrology, where μV/V uncertainty levels are required.

5.1 Performance Metrics

The characterization of ADCs implies the determination of performance metrics in static and dynamic regimes. Therefore, the metrics are divided according to the regime as:

1. Dynamic regime:
    - Total Harmonic Distortion (THD)
    - Signal-to-Noise Ratio (SNR)
    - Signal-to-Noise Ratio plus Distortion (SINAD)
    - Effective Number of Bits (ENOB)
    - Intermodulation Distortion (IMD)
    - Settling time

2. Static regime:

   - Input-Referred Noise
   - Noise-Free Code Resolution

The definition of the enumerated metrics can be found in the IEEE Std. 1241-2001 [7] and IEEE Std. 1057-1994 [6]; as well as in references [77, 78], which are summarized herein for convenience.

5.2 Determination of Performance Metrics in Dynamic Regime

The foregoing sections describe the methods and measurement setup to determine the performance metrics: total harmonic distortion (THD), signal-to-noise ratio (SNR), signal-to-noise ratio plus distortion (SINAD), effective number of bits (ENOB), intermodulation distortion (IMD) and settling time.

5.2.1 Performance Metrics Determination with the Josephson Arbitrary Waveform Synthesizer

The Josephson Arbitrary Waveform Synthesizer (JAWS) is a quantum a.c. voltage standard able to synthesize different kind of waveforms in a wide frequency range [16, 79] including single-tone spectrally pure sinusoidal, or multi-tone sinusoidal signals. The output voltage is calculable and well known which as given by

$$V_J = n_{jj} \frac{f}{K_{J-90}}, \tag{5.1}$$

where n_{jj} is the number of Josephson junctions, f is the microwave signal frequency (typically 70 GHz) and $K_{J-90} = 483597.9$ GHz/V is the Josephson constant.

5.2.1.1 Measurement Setup

The sampling system was connected to the output of the Josephson Arbitrary Waveform Synthesizer system set to an rms amplitude of 5 mV. To avoid spectral leakage when computing the Fourier transform both systems were synchronized by means of the JAWS system clock. Also, the JAWS output was monitored by a PXI-5922 system, connected in parallel with the sampling system. Figure 5.1 shows the measurement setup.

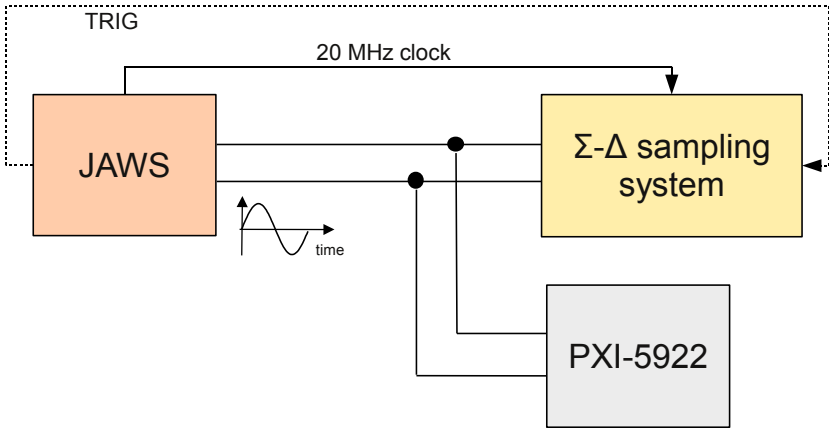


Figure 5.1: Sampling system characterization using a Josephson Arbitrary Waveform synthesizer. Measurement setup diagram.

To reach higher accuracy the oversampling ratio of the Σ-Δ ADC was set to the maximum value of 256. The output data strictly were not corrected for gain, harmonic distortion and offset error of the signal conditioning circuitry to do not mislead the results of this characterization.

This setup was used to measure and determine the total harmonic distortion, signal-to-noise ratio, signal-to-noise ratio plus distortion, effective number of bits and intermodulation distortion.

5.2.2 Total Harmonic Distortion

Total harmonic distortion is the ratio of the rms value of the fundamental to the root-sum-square of its harmonics. Harmonic distortion can be specified with respect to the full-scale input range in units of dBFS (dB relative to full-scale range FSR), or with respect to the input signal amplitude in units of dBc (dB relative to carrier).

If a pure continuous-time sinusoidal waveform of amplitude A_0 and frequency ω_0,

$$x(t) = A_0 \sin(\omega_0 t)\,, \tag{5.2}$$

is applied to a discrete system with non-linear behavior, the output may exhibit distortion. If such system has a transfer function TF modeled by a polynomial as

$$TF\,(x[n]) = a_0 + a_1 x[n] + a_2 x^2[n] + a_3 x^3[n] + a_4 x^4[n] \tag{5.3}$$

Then, the output $y[n]$ of the system is

$$\begin{aligned} y[n] = TF\left(x[n]\right) &= a_0 + a_1 A_0 \sin[\Omega_0\, n] + a_2 A_0^2 \sin^2[\Omega_0\, n] \\ &+ a_3 A_0^3 \sin^3[\Omega_0\, n] + a_4 A_0^4 \sin^4[\Omega_0\, n]. \end{aligned} \tag{5.4}$$

where $\Omega_0 = \omega_0\, T_s$ with T_s the sampling time. Using trigonometric identities equation (5.4) becomes

$$\begin{aligned} y[n] &= \left(a_0 + \frac{a_2 A_0^2}{2} + \frac{3a_4 A_0^4}{8}\right) + \left(a_1 + \frac{3a_3 A_0^2}{4}\right) A_0 \sin[\Omega_0 n] \\ &- \left(a_2 A_0 + a_4 A_0^3\right) \frac{A_0}{2} \cos[2\Omega_0 n] \\ &- \frac{a_3 A_0^3}{4} \sin[3\Omega_0 n] + \frac{a_4 A_0^4}{8} \cos[4\Omega_0 n], \end{aligned} \tag{5.5}$$

as a consequence, harmonic components of the fundamental frequency Ω_0 which are not present in the input signal, appear at the output of the system. The *total harmonic distortion* metric measures the degradation on the input sinusoidal signal.

To characterize the total harmonic distortion (THD) of the ADC (including the input amplifiers) the JAWS was configured to synthesize a single-tone sinusoidal signal which was applied to the system input. Then the THD was calculated as:

$$THD = \frac{\sqrt{\sum_{k=2}^{M} A_k^2}}{A_1} \tag{5.6}$$

or in decibel to carrier (dBc)

$$THD = 20 \log \left(\frac{\sqrt{\sum_{k=2}^{M} A_k^2}}{A_1} \right), \tag{5.7}$$

where A_k is the amplitude of the harmonic k and M is the number of harmonic components for the calculation. To compute the THD the first six harmonic components were taken into account, when possible; otherwise, the harmonic number was reduced to the maximum harmonic measurable in the frequency band of interest. The amplitude of the fundamental frequency and its harmonics were calculated by means of the Fourier transform. As both systems were synchronized using the same clock the coherent sampling conditions were fulfilled, hence no windowing was necessary to apply to the data.

5.2.2.1 Measurement results

Results are presented in tables 5.1-5.2 and in figures 5.2-5.3. Table 5.1 and figure 5.2 show the results for the equivalent sampling rate 4 kHz for an input frequency equal to 500 Hz. Figure 5.3 and table 5.2 depict the results for the equivalent sampling rates 8 kHz, 16 kHz, 32 kHz and 64 kHz for an input signal frequency equal to 1 kHz.

Table 5.1: Total harmonic distortion results

Equivalent Sampling rate (kHz)	f_0 (Hz)	Last Harmonic no. (M)	Amplitude rms (mV)	THD (dBc)
4	500	3	5.838	-92.63

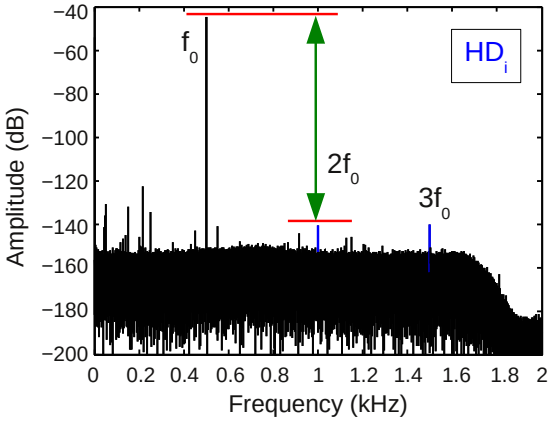
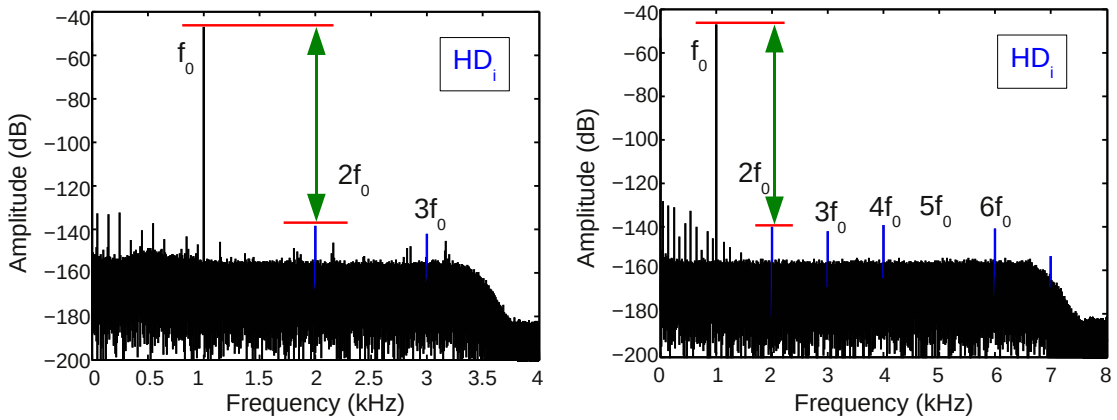


Figure 5.2: Total harmonic distortion for f_o=500 Hz, sampling rate 1024 kHz. Computed THD = -92.63 dBc

Table 5.2: Total harmonic distortion. Results for input signal frequency 1 kHz

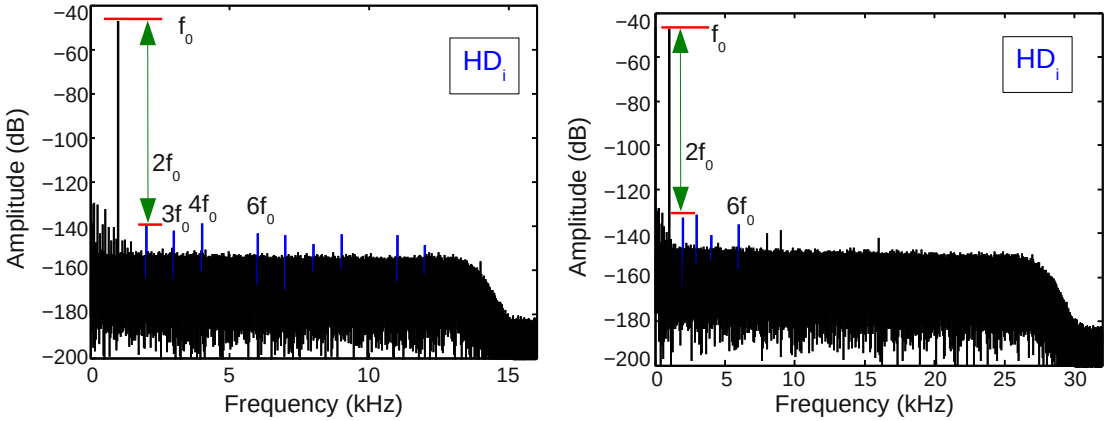
Equivalent sampling rate (kHz)	f_0 (Hz)	Harmonic no. (M)	Amplitude rms (mV)	THD (dBc)
8	1000	3	4.370	-89.98
16	1000	6	4.350	-87.33
32	1000	6	4.355	-87.50
64	1000	6	4.345	-80.80

As reported in the ADC's datasheet [27], the THD for a low amplitude sinusoidal waveform (-60 dBFS) is -75 dBc at an equivalent sampling rate equal to 78 kHz (BW=39 kHz). The measured THD at the maximum equivalent sampling rate (64 kHz with a BW=32 kHz)) was equal to -80.8 dBc. These results indicate that the designed sampling system does



(a) Equivalent sampling rate 8 kHz. Computed THD = -89.98 dBc

(b) Equivalent sampling rate 16 kHz. Computed THD = -87.33 dBc



(c) Equivalent sampling rate 32 kHz. Computed THD = -87.50 dBc

(d) Equivalent sampling rate 64 kHz. Computed THD = -80.80 dBc

Figure 5.3: Total harmonic distortion. Output signals spectra for input signal frequency 1 kHz

not degrade the THD of the ADC at low amplitude level. As the THD usually depends on the signal amplitude it is expected that using a high amplitude test signal, the harmonic distortion on the output signal increases. In addition, when reporting the THD, the amplitude and frequency of the test signal must be specified.

5.2.3 Signal-to-Noise Ratio, Signal-to-Noise Ratio plus Distortion and Effective Number of Bits

This three metrics are determined from the measurement and calculation of the total harmonic distortion and the results are included in table 5.3.

5.2.3.1 Signal-to-Noise Ratio

The signal-to-noise ratio is the ratio of the power of the fundamental to the power of the noise signal (excluding harmonic components of the fundamental and dc) in the frequency band of interest.

5.2.3.2 Signal-to-Noise Ratio plus Distortion

The signal-to-noise ratio plus distortion is calculated combining the SNR and the THD. SINAD is a good indication of the overall dynamic performance of the ADC because it includes noise and distortion. Therefore, the SNR is replaced by the SINAD in order to calculate the effective number of bits.

5.2.3.3 Effective Number of Bits

The effective number of bits defines the usable resolution of the Σ-Δ ADC. The ENOB is calculated from the SINAD by replacing the SNR in equation (2.14), thus

$$ENOB = \frac{SINAD - 1.76}{6.02}. \tag{5.8}$$

When the input signal amplitude A_0 is below the ADC full scale, equation (5.8) has to be scaled to the ADC full scale by a factor $K = 20\ \log(FS/A_0)$, then the ENOB is computed by

$$ENOB = \frac{SINAD - 1.76 + K}{6.02}. \tag{5.9}$$

5.2.3.4 Measurement Results

From the THD follows the calculation of the SNR, the SINAD (including harmonic distortion) and the ENOB scaled to an input full scale of 1 V as equation (5.9 states). Table 5.3 shows the results.

Table 5.3: SNR, SINAD and ENOB results

Equivalent sampling rate (kHz)	f_0 (Hz)	Amplitude rms (mV)	noise rms (μV)	SNR (dBc)	noise+HD (μV)	SINAD (dBc)	ENOB (bits)
4	500	5.843	4.58	62.12	4.58	62.11	16.94
8	1000	4.382	3.63	61.63	3.64	61.62	17.28
16	1000	4.381	2.90	63.57	2.91	63.55	17.60
32	1000	4.376	3.86	61.09	3.86	61.08	17.19
64	1000	4.371	7.24	55.61	7.26	55.60	16.28

The ENOB can be compared with a commercial equipment. The ENOB at the maximum equivalent sampling rate of 64 kHz was determined as 16.28 bits. Using equation (5.8) to find the SINAD, it results in

$$SINAD = 6.02\,ENOB + 1.76\,\text{dB} = 99.8\,\text{dB}\,, \tag{5.10}$$

the SINAD of a commercial digital voltmeter based on an integrating ADC (IADC), the Agilent 3458A, is equal to 93.9 dB which is equivalent to an ENOB = 15.3 bits at a sampling rate equal to 50 kHz with an integration time of 10 μs as reported in [80]. These results confirm that the designed sampling system resolution is ≈ 1 bit higher than the IADC.

5.2.4 Intermodulation Product Distortion

The intermodulation product distortion IMD is the ratio of power of the intermodulation products to the total power of the original frequencies, as a result of two tones simultaneously applied to the ADC input. IMD is either given in units of dBc or dBFS.

If a two-tone sinusoidal signal modeled as

$$x(t) = A_0 \sin(\omega_1 t) + A_0 \sin(\omega_2 t) \tag{5.11}$$

is applied to the system with a transfer function given by equation (5.3), the discrete time output $y[n]$ contains high order harmonic components and inter-frequency products, and

becomes [81]

$$
\begin{aligned}
y[n] &= a_0 + a_2 A_0^2 + \frac{9 a_4 A_0^4}{4} - \left(\frac{1}{2} a_2 A_0^2 + 2 a_4 A_0^4\right) \cos[2\Omega_1 n] \\
&+ \frac{1}{8} a_4 A_0^4 \cos[4\Omega_1 n] - \left(\frac{1}{2} a_2 A_0^2 + 2 a_4 A_0^4\right) \cos[2\Omega_2 n] \\
&+ \frac{1}{8} a_4 A_0^4 \cos[4\Omega_2 n] + a_2 A_0^2 \cos[(\Omega_1 - \Omega_2) n] - a_2 A_0^2 \cos[(\Omega_1 + \Omega_2) n] \\
&+ 3 a_4 A_0^4 \cos[(\Omega_1 - \Omega_2)] - 3 a_4 A_0^4 \cos[(\Omega_1 + \Omega_2)] \\
&+ \frac{1}{2} a_4 A_0^4 \cos[(3\Omega_1 + \Omega_2) n] - \frac{1}{2} a_4 A_0^4 \cos[(3\Omega_1 - \omega_2) n] \\
&- \frac{1}{2} a_4 A_0^4 \cos[(\Omega_1 - 3\Omega_2) n] + \frac{1}{2} a_4 A_0^4 \cos[(\Omega_1 + 3\omega_2) n] \\
&+ \frac{3}{4} a_4 A_0^4 \cos[(2\Omega_1 - 2\Omega_2) n] + \frac{3}{4} a_4 A_0^4 \cos[(2\Omega_1 + 2\omega_2) n] \\
&+ \left(a_1 A_0 + \frac{9}{4} a_3 A_0^3\right) \sin[\Omega_1 n] + \left(a_1 A_0 + \frac{9}{4} a_3 A_0^3\right) \sin[\Omega_2 n] \\
&- \frac{1}{4} a_3 A_0^3 \sin[3\Omega_1 n] - \frac{1}{4} a_3 A_0^3 \sin[3\Omega_2 n] \\
&- \frac{3}{4} a_3 A_0^3 \sin[(\Omega_1 - 2\Omega_2) n] + \frac{3}{4} a_3 A_0^3 \sin[(2\Omega_1 - \Omega_2) n] \\
&- \frac{3}{4} a_3 A_0^3 \sin[(\Omega_1 + 2\Omega_2) n] + \frac{3}{4} a_3 A_0^3 \sin[(2\Omega_1 + \Omega_2) n] \,, \qquad (5.12)
\end{aligned}
$$

where $\Omega_1 = \omega_1 T_s$ and $\Omega_2 = \omega_2 T_s$ with T_s the sampling time.

As equation (5.12) states, the nonlinear transfer function TF of the system, apart from harmonic distortion, generates inter-frequency products at frequency $k\,\Omega_1 \pm j\,\Omega_2$ with k, j integers. $q = |k| + |j|$ determines the order of the inter-frequency product. From equation (5.12) it is possible to identify the amplitude of the inter-frequency products $A(k\,\Omega_1 \pm j\,\Omega_2)$ as

$$
\begin{aligned}
A(\Omega_1 \pm \Omega_2) &= a_2 A_0^2 \\
A(2\,\Omega_1 \pm \Omega_2) &= A(\Omega_1 \pm 2\,\Omega_2) = \frac{3}{4} a_3 A_0^3 \\
A(3\,\Omega_1 \pm \Omega_2) &= A(\Omega_1 \pm 3\,\Omega_2) = \frac{1}{2} a_4 A_0^4 \\
A(2\,\Omega_1 \pm 2\,\Omega_2) &= \frac{3}{4} a_4 A_0^4 \,.
\end{aligned}
$$

The *intermodulation distortion* metric specifies these inter-frequency products.

5.2.4.1 Measurement Results

To determine the intermodulation product distortion (IMD) the JAWS was configured to synthesize a two-tones sinusoidal signal which was applied to the system input. In this test the intermodulation products $|kf_1 \pm jf_2|$ with $k, j = 1, 2 \text{ and } 3$ were computed by the following relation [82]:

$$IMD_q = \frac{\max\{A^2(|kf_1 + jf_2|)\}}{\min\{A^2(f_1), A^2(f_2)\}}, \tag{5.13}$$

where $A(kf_1)$ is the amplitude of the frequency component kf_1, likewise for the index j and $q = |k| + |j|$ is the intermodulation order. This equation (5.13) represents the worst case since the IMD is computed as the ratio between the maximum amplitude of the distortion product to the minimum amplitude of the two-tones signal applied to the system. The IMD expressed in dBc is:

$$IMD_q = 20 \log\left(\frac{\max\{A(|kf_1 + jf_2|)\}}{\min\{A(f_1), A(f_2)\}}\right), \tag{5.14}$$

Table 5.4 shows the results of the second order to the forth order intermodulation products. The amplitude of the frequency components were calculated from the Fourier transform of the measured data without windowing as in the case of the THD.

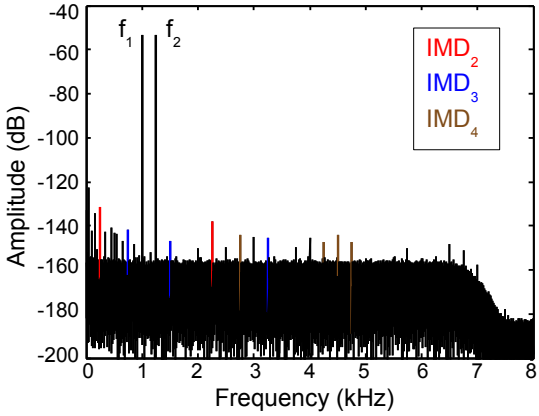
Table 5.4: Intermodulation distortion, $f_1 = 1000$ Hz, $f_2 = 1250$ Hz

Equivalent sampling rate (kHz)	f_i (Hz)	Amplitude rms (mV)	IMD_2 (dBc)	IMD_3 (dBc)	IMD_4 (dBc)
16	1000	2.175	-84.67	-88.64	-89.70
	1250	2.180			
32	1000	2.178	-81.02	-94.09	-89.44
	1250	2.185			
64	1000	2.173	-76.67	-82.67	-91.36
	1250	2.168			

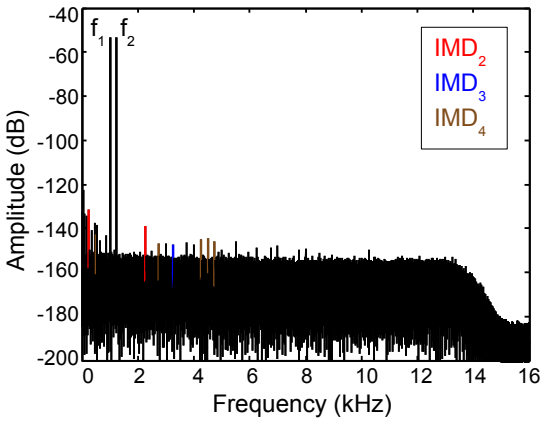
Figure 5.4 depicts the output signal spectra of the IMD measurements for different sampling rates.

5.2.5 Settling Time

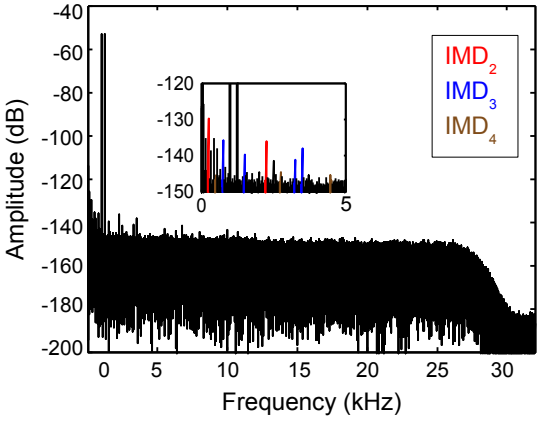
An important parameter for sampling systems is the settling time, defined as the time required by its readout to converge to ± 0.01 % of the final value in response to a step change at its input. This parameter is vital when sampling rapidly changing signals,



(a) Equivalent sampling rate 16 kHz.



(b) Equivalent sampling rate 32 kHz.



(c) Equivalent sampling rate 64 kHz.

Figure 5.4: Intermodulation distortion. Output signals spectra for IMD calculation $f_1 = 1$ kHz, $f_2 = 1.25$ kHz. The inset in (c) depicts the IMD_i at the equivalent sampling rate 64 kHz.

arbitrary waveforms which appear in power quality, and in multiplexed systems. For Σ-Δ ADCs, this parameter depends on the decimation rate selected, which determines the order of the Σ-Δ ADC internal digital filters [78, 83].

5.2.5.1 Measurement Results

The Josephson waveform synthesizer (JWS) is capable to generate stepwise approximated waveforms. Its accuracy and intrinsic noiseless and non-drift properties can be exploited to determine the settling time of the Σ-Δ ADC. Because of that, the transition between two adjacent steps of a stepwise approximated waveform can be used to measure the sampling system settling time provided that the steps duration is long enough to allow settling of the system response.

The response of the sampling system to a transition between two adjacent quantum plateaus, as illustrated in figure 5.5, results in a settling time of 24 samples. The response of the analog input amplifiers is included in this time. The length of the overall ADC

internal decimation filters was 55, which corresponds to a decimation factor of 256. Table 6 in reference [27]) specifies the group delay of the digital filters in unit of time for different sampling rates and decimation factors. The row with which the length of the digital filters was obtained is transcribed here for clarity The filters group delay (GD) is equal to the

Table 5.5: AD7763 decimation filters default configuration

Clock frequency	Filters			Computation delay	Filters delay	Equivalent f_s
	FIR 1	FIR 2	FIR 3			
20 MHz	4	32	2	4.65 μs	346.8 μs	78.125 kHz

computation delay plus the filters delay according to reference [27]. From table 5.5 results

$$\mathrm{GD} = 4.65\,\mu\mathrm{s} + 348.8\,\mu\mathrm{s} = 351.45\,\mu\mathrm{s}\,.$$

The group delay can be converted to number of samples by

$$\mathrm{GD}_{samples} = 351.45\,\mu\mathrm{s} \times 78.125\,\mathrm{kHz} = 27.5\,\mathrm{samples}\,.$$

Then, it follows that the overall filter length is 2×27.5 samples $= 55$ samples.

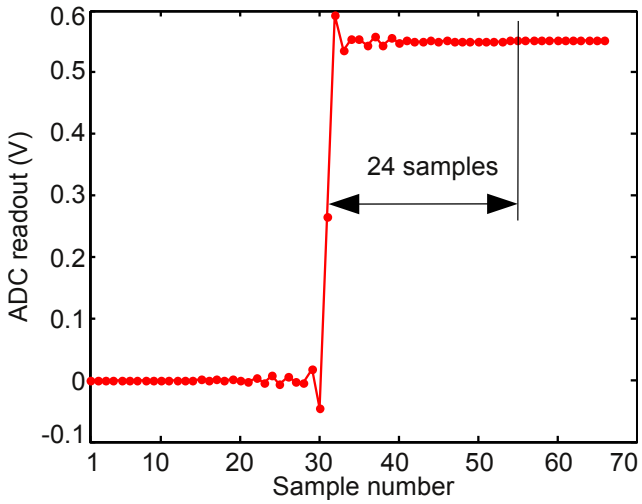


Figure 5.5: Overall system settling time

The overall filter length remains constant for the different sampling rates, since it depends on the decimation factor. Therefore, converting the number of samples to time results in the settling times as is shown in table 5.6.

These results can be compared with an integrating ADC used in a digital voltmeter (DVM), such as the Agilent 3458A. The settling time of the DVM for the DCV sampling mode is 20 μs at the input ranges 1 V and 10 V [84]. As can be seen, the settling time

Table 5.6: Settling times as a function of sampling rates

Sampling Rate (kHz)	Equivalent Sampling rate (kHz)	Settling time	
		no. of samples	(ms)
1024	4		6
2048	8		3
4096	16	24	1.5
8192	32		0.75
16384	64		0.375

in a Σ-Δ ADC is higher, as a consequence the settling time is a limiting factor when sampling arbitrary waveforms or in precision measurements. The effect of the settling time is described in section 7.1.2 when measuring sinusoidal signals.

5.3 Determination of Performance Metrics in Static Regime

Two performance metrics were determined using a dc quantum plateau of the Josephson waveform synthesizer, the input-referred noise and the noise-free code resolution.

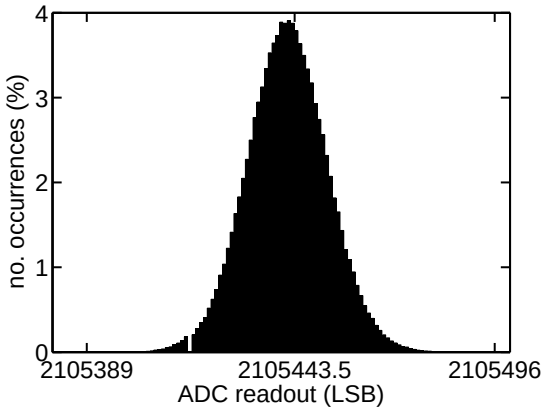
5.3.1 Input-Referred Noise

The input-referred noise or code transition noise in ADC is any deviation between the output digital code with a dc, noise-free, input signal [85].

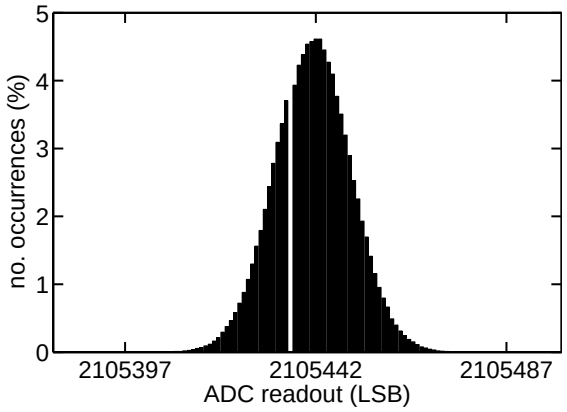
The ADC internal circuits produce a certain amount of root-mean-square (rms) noise e_{rms}. In Σ-Δ ADCs, this depends mainly on noise in amplifiers and sampled thermal noise kT/C [4], where k is the Boltzmann constant, T is the absolute temperature and C is the input capacitance mentioned in 3.2.2.2. For the complete system, additional contributions due to thermal noise from the operational amplifiers and quantization noise from the ADC must also be considered.

5.3.1.1 Measurement Results

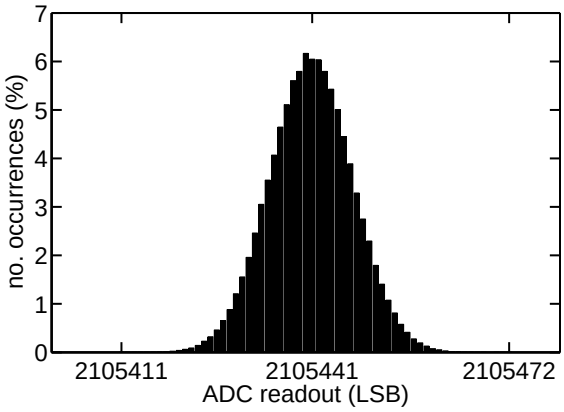
To measure the input-referred noise or *code-transition noise*, a single JWS dc plateau equal to 1 V was applied to the sampling system input and then the histogram of the ADC output codes was computed. The normalized histograms, centered around the median value, for the different equivalent sampling rates are shown in figure 5.6 and the results are summarized in table 5.7.



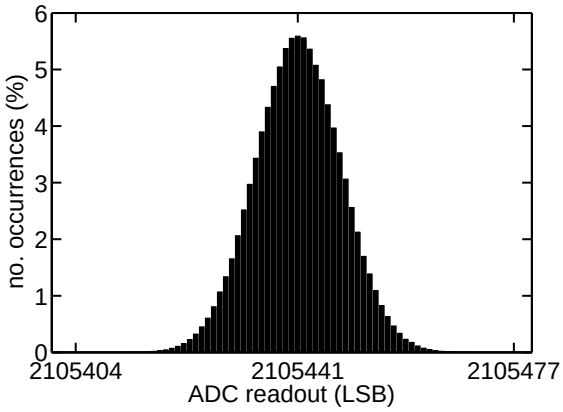
(a) Equivalent sampling rate 4 kHz



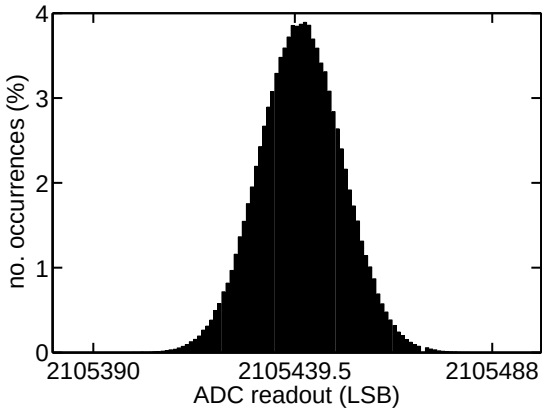
(b) Equivalent sampling rate 8 kHz



(c) Equivalent sampling rate 16 kHz



(d) Equivalent sampling rate 32 kHz



(e) Equivalent sampling rate 64 kHz

Figure 5.6: ADC readout histograms for an input JWS dc plateau equal to 1 V

The resulting histograms are a measure of the code distribution for this particular dc voltage and follow nearly a normal distribution, as can be seen from figure 5.6. Therefore, the standard deviation represents the rms value of the sum of all noise sources e_{rms} [85]. The worst case was measured at the equivalent sampling rate of 64 kHz, resulting in a

Table 5.7: Histograms results for a JWS dc plateau equal to 1 V

	Equivalent Sampling rate				
	4 kHz	8 kHz	16 kHz	32 kHz	64 kHz
minimum (LSB)	2105389	2105397	2105411	2105404	2105390
maximum (LSB)	2105496	2105487	2105472	2105477	2105488
median (LSB)	2105443.5	2105442	2105441	2105441	2105439.5
e_{rms} (LSB)	10.05	9.26	6.35	6.82	10.25

rms noise equal to 10.25 LSBs, which corresponds to rms voltage equal to 1.2 μV. The noise limits the resolution of the Σ-Δ ADC, as it will be explained below.

5.3.2 Noise-Free Code Resolution

The noise-free code resolution is the number of bits of resolution beyond which it is impossible to distinguish between individual codes [78, 85]. It defines the usable number of bits of the ADC and it is limited by the input-referred noise. This metric is associated with high resolution Σ-Δ ADC.

From the input-referred noise e_{rms} the maximum SNR for a N-bits ADC can be calculated as

$$SNR\Big|_{max} = \frac{2^N}{e_{rms}(LSBs)}\,. \tag{5.15}$$

Then the *effective resolution* in bits can be obtained by calculating the base-2 logarithm of equation (5.15)

$$\text{Effective resolution} = \log_2\left(\frac{2^N}{e_{rms}}\right), \tag{5.16}$$

From the effective resolution follows that the noise-free code resolution can be calculated by replacing the rms noise e_{rms} with the peak-to-peak noise $e_{p-p} = 6.6 \times e_{rms}$ in equation (5.16), hence

$$\begin{aligned} \text{Noise-free code resolution} &= \log_2\left(\frac{2^N}{\text{peak-to-peak input noise}}\right) \\ &= \log_2\left(\frac{2^N}{6.6\,e_{rms}}\right), \end{aligned} \tag{5.17}$$

From equation (5.16) and (5.17) follows the relation between the noise-free code res-

olution and the effective resolution which is given by

$$\begin{aligned} \text{Effective resolution} &= \text{Noise-free code resolution} + \log_2(6.6) \\ &\approx \text{Noise-free code resolution} + 2.7\,\text{bits}\,. \end{aligned} \tag{5.18}$$

As it is stated by equation (5.18) the effective resolution differs form the noise-free code resolution in 2.7 bits.

5.3.2.1 Measurement Results

The noise-free code resolution and the effective resolution obtained for the Σ-Δ ADC used in this thesis are given in table 5.8.

Table 5.8: Noise-free code resolution and effective resolution for the different equivalent sampling rates

Equivalent sampling rate (kHz)	Noise-free code resolution (bits)	Effective resolution (bits)
4	17.95	20.67
8	18.07	20.79
16	18.61	21.33
32	18.51	21.23
64	17.92	20.64

From the noise-free code resolution results shown in table 5.8 it can be concluded that the ADC resolution is not degraded by to the associated signal conditioning circuit (input buffer and FDA) and the system clock.

It is important to point out the difference between the effective resolution (or the noise-free code resolution) and the effective number of bits (ENOB). The effective resolution measures the attainable ADC resolution, while the ENOB expresses the SNR plus harmonic distortion in unit of bits.

The rms noise-free code resolution e_{rms}, relative to the system full-scale, has been considered as resolution uncertainty since it measures the uncertainty with which a single ADC code or a sample value can be identified.

Chapter 6

System Model Parameter Identification

In chapter 4 the proposed model to post-compensate the sampling system readouts has been described. The model describes or predicts the behavior of the sampling system relating its input/output signals by means of a transfer function. This function is constructed from observing the system response to a well-known input signal. The process of building this transfer function is called identification. If this is the case, it is referred as to parametrize the transfer function with a set of a finite number of parameters. This chapter describes the parameter identification of the sampling system model based on a sigma-delta analog-to-digital converter using a Josephson waveform synthesizer. The methods and measurement procedures described herein allow the determination of the performance metrics such as non-linearity, gain and offset of the system when sampling alternating signals with accuracies at the μV/V level. Additional compensations to apply to the sampled data are also described, the compensation for the sample-and-hold of the analog-to-digital converter and the correction for the frequency response of the anti-aliasing low-pass filter. With all these compensation the input signal can be reconstructed in order to calculate for instance, the root-mean-square (rms) value. A description of the calculation of rms value from the reconstructed signal is also included. Finally, an uncertainty evaluation of the system is presented to complete the characterization of the capabilities of the sampling system.

6.1 The System Model

As it has been described in chapter 4 the proposed model to post-compensate the system readouts for non-linearities and distortion is the Hammerstein model as illustrated in figure 6.1. The identification is divided in two parts: i) the non-linear block and ii) the linear block compensation.

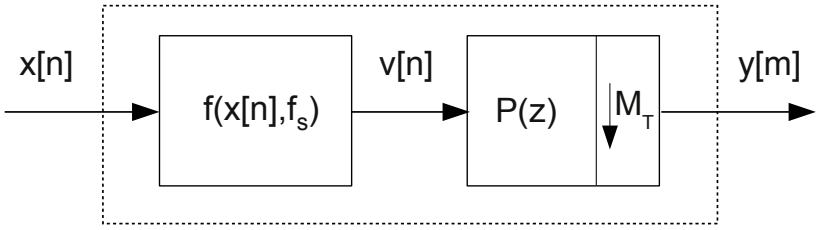


Figure 6.1: Simplified block diagram of the sampling system model, where f(x[n], f_s) represents the non-linear block while P(z) represents the linear block.

6.2 Non-linear Block Parameter Identification

The parameters of the non-linear block with a transfer function $f(x[n], f_s)$, relating the output data codes to the input voltages was obtained by means of the Josephson Waveform Synthesizer (JWS). The intrinsic characteristics of noise-free, drift-free and the inherent accuracy make the JWS a powerful tool when characterizing sampling systems as has been reported in [1, 86] where the JWS has been used to characterize integrating ADCs as samplers.

6.2.1 The Josephson Waveform Synthesizer

Voltage standards based on the Josephson effect [87] have been used since 1990 for national metrology institutes (NMI) to realize the unit of voltage. When a Josephson array with n_{jj} Josephson junctions is biased by a constant current and irradiated by a microwave signal of frequency f (typically 70 GHz) produces a constant dc voltage V_J determined by

$$V_J = n_{jj} \frac{f}{K_{J-90}}, \tag{6.1}$$

where $K_{J-90} = 483597.9$ GHz/V is the Josephson constant. The uncertainty on V_J is $u(V_J) \approx 1$ part in 10^{10}, this value makes the Josephson waveform synthesizer an absolute voltage reference for the sampling system under characterization.

Advances in the development of Superconductor-Normal-Superconductor (SNS) [88] and Superconductor-Isolator-Normal-Isolator-Superconductor (SINIS) [89] Josephson junctions which can be dc biased by a driving current have opened up new applications in ac metrology [3, 90, 91].

The Josephson Waveform Synthesizer uses these kind of Josephson arrays with which it is capable to synthesize stepwise approximated waveforms with amplitudes in ± 10 V range.

6.2.1.1 Stepwise Approximated Waveform

The JWS is capable to synthesize stepwise approximated waveform, depending on the number of steps and the voltage difference between them, the waveform can approach triangle or sinusoidal waveforms. A stepwise approximated triangle waveform using 16 steps per period synthesized by the JWS is depicted in figure 6.2. The amplitude of each step is given by equation (6.1). This stepwise triangle waveform was employed to

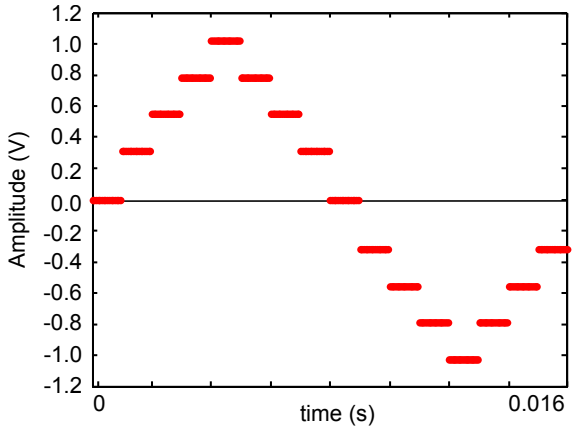


Figure 6.2: 16-steps per period stepwise approximated triangle waveform with amplitude ± 1 V and frequency 62.5 Hz

characterize the Σ-Δ sampling system.

6.2.1.2 Measurement Setup

A scheme of the measurement setup is shown in figure 6.3. The output of the Josephson

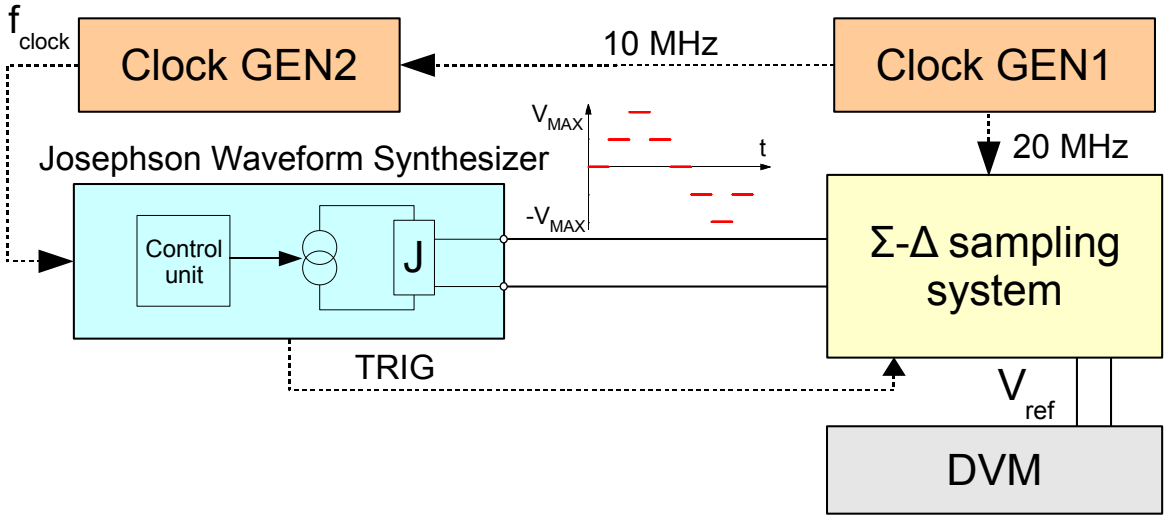


Figure 6.3: Measurement setup for the system model parameter identification

waveform synthesizer was connected to the Σ-Δ sampling system. In order to synchronize

the generation and sampling, an external clock generator (Clock GEN1) was used as main clock. A second clock generator (Clock GEN2), which was locked in frequency to the main clock, provided the clock signal to the JWS system. This arrangement allowed the modification of the clock frequency of the JWS system so as to change externally the frequency of the signal to synthesize, keeping the synchronization provided that the signal frequency is an integer multiple of the clock frequency. During the test, the JWS was configured to generate a stepwise triangle waveform using 8 or 16 steps per period, with amplitude ±1 V and a frequency range from 7.8125 Hz to 62.5 Hz. The Σ-Δ sampling system sampled these waveforms at five different equivalent sampling rates 4 kHz, 8 kHz, 16 kHz, 32 kHz and 64 kHz. The ADC was configured with a decimation rate set to the maximum value of 256 in order to obtain the best achievable performance. Table 6.1 summarizes the measurement parameters.

Table 6.1: Measurement parameters

Equivalent	JWS Signal	
Sampling rate	freq.	no. steps
4 kHz	7.8125 Hz	8
8 kHz	7.8125 Hz	16
16 kHz	15.625 Hz	16
32 kHz	31.25 Hz	16
64 kHz	62.5 Hz	16

With this configuration, the number of samples per period and the number of samples per step were equal to 1024 and 64, respectively, for sampling rates from 8 kHz to 64 kHz. However, for the lower sampling rate (4 kHz), the number of samples per step was 64 (the same as before), but the number of samples per period was 512 samples. This configuration allows to remove the transients of the ADC digital filters from the readouts, which is of utmost importance to avoid wrong results, and this configuration is statistically equivalent for the different ADC sampling rates. The total number of samples acquired on each measurement were the maximum capacity of the Σ-Δ sampling system internal buffer, equal to 524288 samples.

In addition, a high resolution digital voltmeter model Agilent-3458A, DVM, was used to monitor the Σ-Δ ADC voltage reference V_{ref} during the measurements.

6.2.2 Polynomial Transfer Function $f(x[n])$

In section 3.2 has been described and confirmed by the results characterization with the JAWS reported in sections 5.2.2 and 5.2.4, that the sampling system produces harmonic distortion due to non-idealities (amplifiers, component mismatches). The magnitude up

to the 4^{th} order harmonic are the ones which may introduce deviations when measuring alternating signal parameters, such as root-mean-square voltage. Therefore, the transfer function $f(x[n])$ of the non-linear block of the Hammerstein model is a fourth order polynomial as

$$f(x[n]) = a_4x^4[n] + a_3x^3[n] + a_2x^2[n] + a_1x[n] + a_0\,, \tag{6.2}$$

in which $x[n]$ is the input signal to the Σ-Δ sampling system and a_i are the polynomial coefficients.

In order to obtain the polynomial coefficients a_i, the Σ-Δ sampling system readouts were processed as follows:

1. The transient response of the digital decimation filters of the Σ-Δ ADC were removed from each quantum plateau. Then, the remaining samples were averaged so that one single point per plateau was obtained;

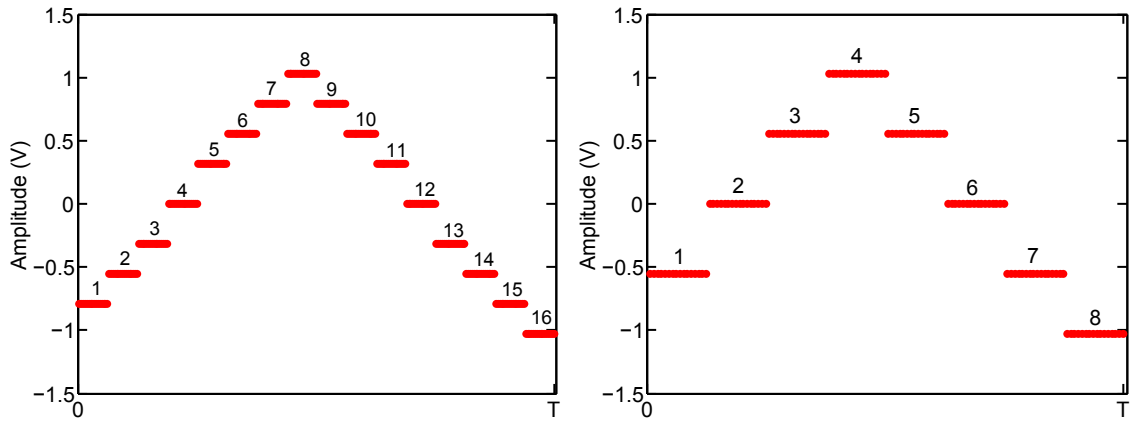
2. then, the differences between these averaged points with their corresponding 0 V in the signal were calculated over the corresponding period, following the method described in [90]. As a result, the readouts were compensated from thermal e.m.f. and drift;

3. the Allan deviation was then calculated to determine the observation time τ over which the system noise is white, i.e. the observation time in which the Allan deviation decreases.

4. next, from the observation time τ, the corresponding number of periods L over the total number of acquired periods M_P were determined. As a consequence, the total number of periods were split into $Q = \lfloor M_P/L \rfloor$ frames of L periods each one ($\lfloor\cdot\rfloor$ denotes the floor function);

5. finally, a fourth order polynomial least squares fit relative to the input voltage V_J was performed to find the polynomial $f(x[n])$ (equation (6.2)) of the Hammerstein model. Then, the polynomial $f(x[n])$ was inverted to obtain the coefficients b_i of the post-correction polynomial $r(v[n])$ as has been described in section 4.3.

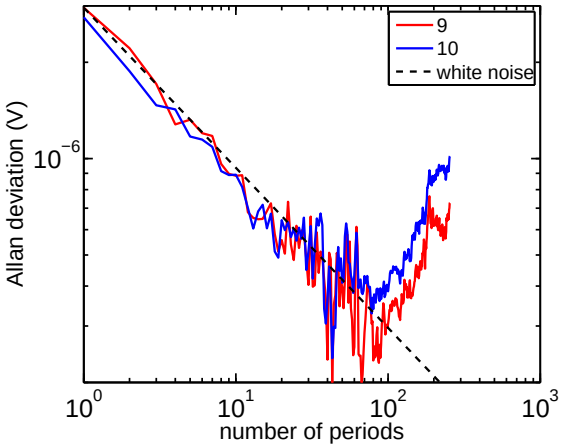
As it has been stated in item 4 the number of periods L depends on the results of the Allan deviation. The Allan deviation plots are depicted in figures 6.5 and 6.6. These plots include only the limiting curves from the set of 16 or 8 plateaus of the JWS signal. The number of periods L for each equivalent sampling rate were determined when the Allan deviation reaches the $1/f$ noise floor, this limit indicates that the measured data are uncorrelated.



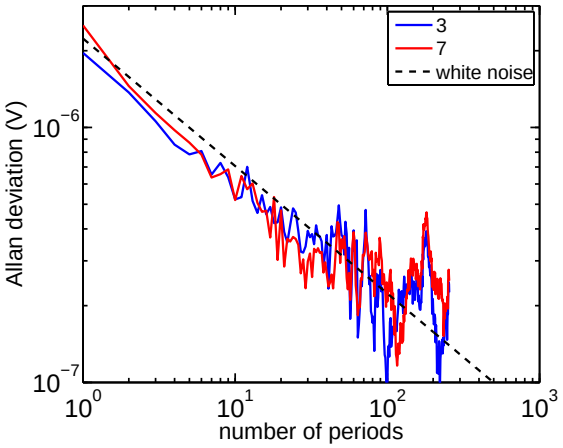
(a) 16-steps

(b) 8-steps

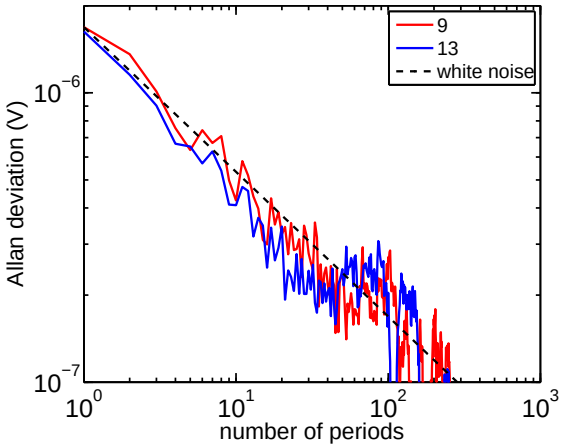
Figure 6.4: JWS signal representation of the steps for the Allan deviation calculations



(a) Equivalent sampling rate 64 kHz

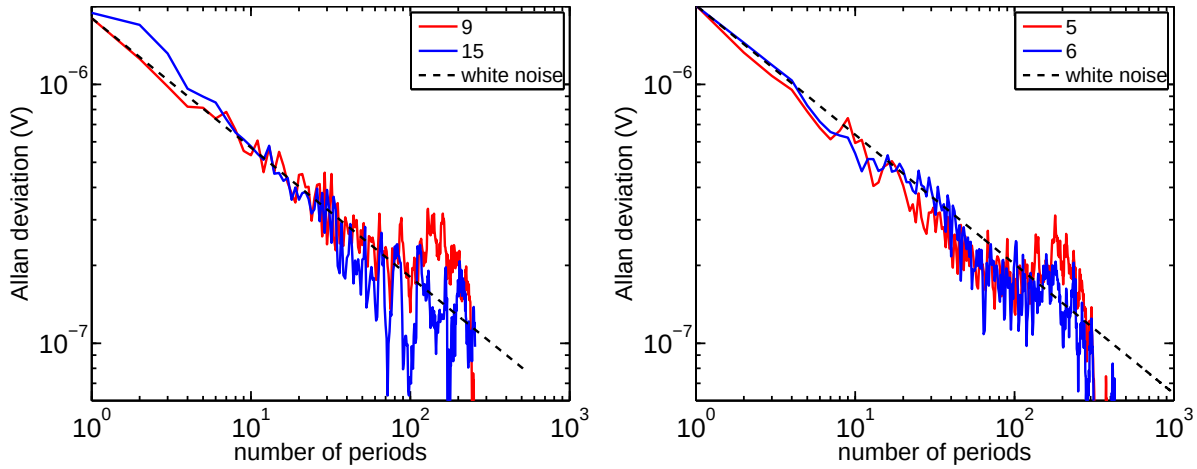


(b) Equivalent sampling rate 32 kHz



(c) Equivalent sampling rate 16 kHz

Figure 6.5: Allan Deviation plots for equivalent sampling rates 64 kHz, 32 kHz and 16 kHz



(a) Equivalent sampling rate 8 kHz

(b) Equivalent sampling rate 4 kHz

Figure 6.6: Allan Deviation plots for equivalent sampling rates 8 kHz and 4 kHz

The Allan deviation results show that the observation time is within the interval from 0.64 s to 25.6 s depending on the equivalent sampling rate. At the equivalent sampling rates 64 kHz, 32 kHz and 16 kHz (figure 6.5) the system reaches the $1/f$ noise floor after 40 periods which correspond to an observation time of 0.64 s, 1.28 s and 2.56 s, respectively. The highest equivalent sampling rate (64 kHz) shows a linear drift after 80 periods as can be seen in figures 6.5(a) which corresponds to an observation time equal to 1.28 s. At the equivalent sampling rates 8 kHz and 4 kHz (figure 6.6) the system reaches the $1/f$ noise floor after 200 periods resulting in an observation time of 25.6 s.

With these results, it is possible to estimate the lower attainable uncertainty when computing the set of coefficients a_i of the polynomial $f(\cdot)$. Extending the observation time further than the $1/f$ noise floor will introduce correlation between the measured data. The Allan deviation results are summarized in table 6.2.

Table 6.2: Allan deviation results

JWS signal frequency (Hz)	Equivalent sampling rate (kHz)	Total no. of periods M	No. of periods L	Observation time τ (s)	No. of frames Q
62.5	64	512	40	0.64	12
31.25	32	512	40	1.28	12
15.625	16	512	40	2.56	12
7.8125	8	512	200	25.6	2
7.8125	4	1024	200	25.6	5

To obtain the coefficients a_i of the polynomial $f(\cdot)$, a least squares fitting method relative to the input voltage V_J was performed on each frame Q, as indicated in section 4.4.1, and then were in turn averaged. From this result, the coefficients b_i of the post-

compensating inverse polynomial $r(\cdot)$ were calculated at each sampling rate so that

$$r(f(x[n])) \approx \mathbf{1}\,.$$

Hence there is a set of five polynomials. These set of coefficients are listed in table 6.3.

Table 6.3: Polynomial coefficients and the corresponding Type-A uncertainty (u)

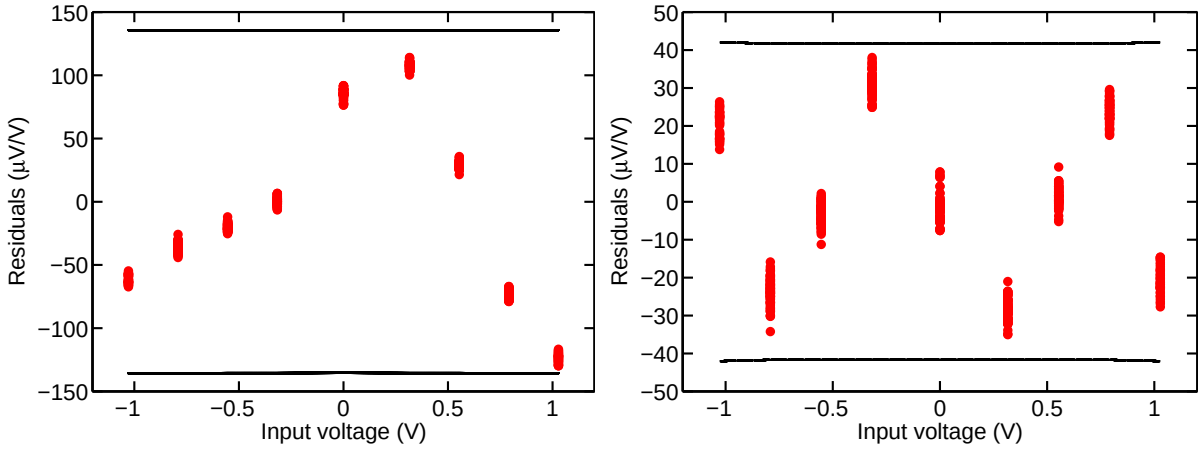
Equivalent sampling rate	coefficients				
	b_4 ($1/V^3$)	b_3 ($1/V^2$)	b_2 ($1/V$)	b_1 (V/V)	b_0 (V)
64 kHz	-135.18 10^{-6}	134.01 10^{-6}	310.96 10^{-6}	1.00460508	2.92 10^{-6}
u	7.84 10^{-6}	4.26 10^{-6}	8.30 10^{-6}	3.14 10^{-6}	1.63 10^{-6}
32 kHz	-38.81 10^{-6}	54.11 10^{-6}	87.06 10^{-6}	1.00265017	5.04 10^{-6}
u	2.04 10^{-6}	1.11 10^{-6}	2.17 10^{-6}	8.20 10^{-7}	4.28 10^{-7}
16 kHz	-13.31 10^{-6}	14.02 10^{-6}	24.97 10^{-6}	1.00154515	1.77 10^{-6}
u	9.60 10^{-7}	5.23 10^{-7}	1.02 10^{-6}	3.88 10^{-7}	2.03 10^{-7}
8 kHz	-2.80 10^{-6}	1.50 10^{-6}	6.80 10^{-6}	1.00119768	4.02 10^{-7}
u	3.11 10^{-7}	1.69 10^{-7}	3.31 10^{-7}	1.26 10^{-7}	6.56 10^{-8}
4 kHz	-3.18 10^{-8}	-1.82 10^{-6}	1.43 10^{-6}	1.00115397	4.5 10^{-8}
u	4.62 10^{-7}	2.17 10^{-7}	5.41 10^{-7}	1.87 10^{-7}	1.01 10^{-7}

The non-linearities, up to the order of the polynomial, are compensated applying the polynomial $r(\cdot)$ to the ADC readouts. This compensation can be observed and analyzed on the residual plots of the fitting process [76]. The residuals (the difference between the ADC readouts and the fitted data), namely

$$\epsilon = x[n] - r(v[n])\,, \tag{6.3}$$

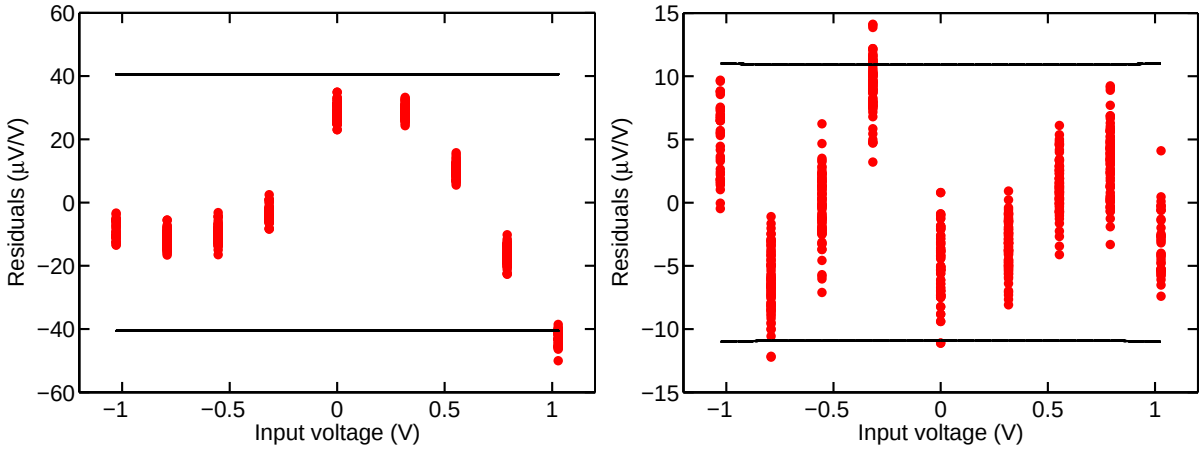
are shown from figure 6.7 to figure 6.11. On figures 6.7(a)-6.11(a) the residuals of a linear fit are shown where the non-linear behavior of the system is clearly seen. On figure 6.7(b)-6.11(b) the residuals of the polynomial fit are depicted in which can be observed a random distribution of the residuals around 0 μV/V, indicating that the polynomial $r(\cdot)$ compensates the sampling system from its non-linearities. These plots also show the prediction interval (see equation 4.26) with a 95 % confidence level.

The non-linearities increase as the equivalent sampling rate increases. This effect is produced by the imperfections as described in section 3.2. Mainly, mismatch in gain and phase of the input buffer and FDA, amplifiers limited bandwidth and Σ-Δ ADC modulators finite gain bandwidth and slew rate contribute to the overall system non-linearity. The Σ-Δ ADC is built using switched-capacitor (SC) circuits. SC circuits exhibit non-linear behavior which produce harmonic distortion as the frequency of oper-



(a) Linear fit (b) Polynomial fit

Figure 6.7: Least squares fitting residuals in (μV/V) relative to 1 V for a k=2 (95 %) prediction interval. (a) Linear fit, (b) Polynomial fit. Equivalent sampling rate 64 kHz



(a) Linear fit (b) Polynomial fit

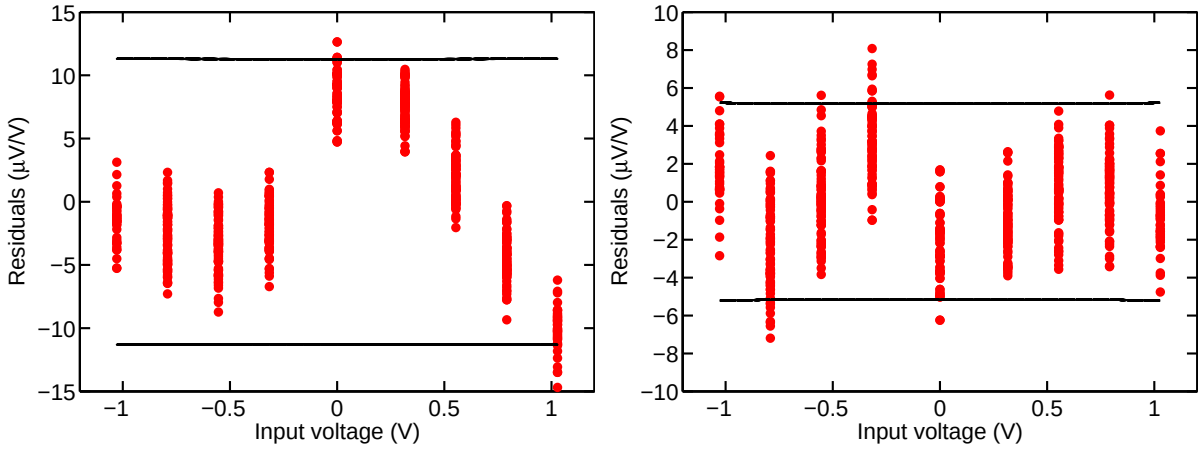
Figure 6.8: Least squares fitting residuals in (μV/V) relative to 1 V for a k=2 (95 %) prediction interval. (a) Linear fit, (b) Polynomial fit. Equivalent sampling rate 32 kHz

ation increases [51].

6.3 Linear Block Compensation

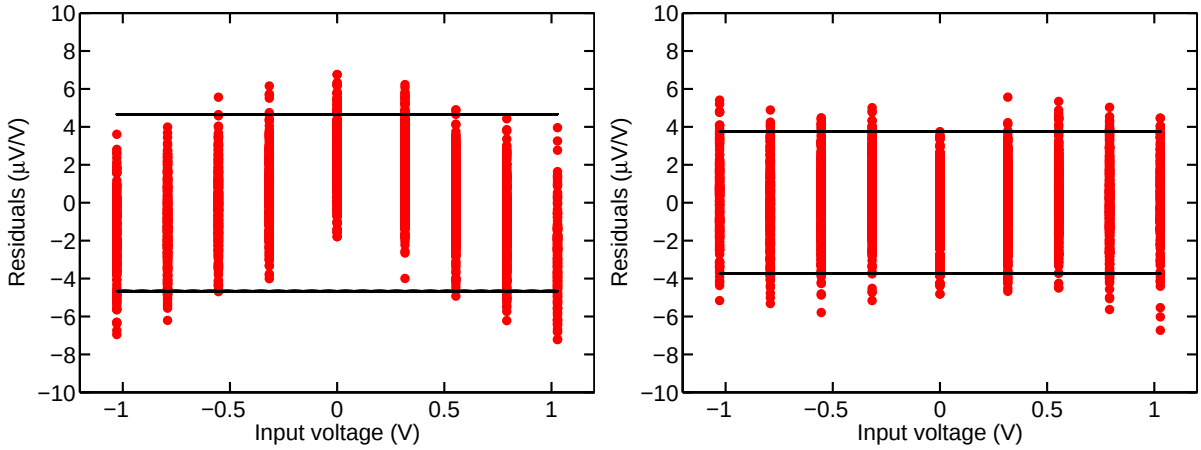
In a Σ-Δ ADC the low resolution high sampling rate output of the quantizer is converted to a high resolution output at the Nyquist sampling rate [22]. This is accomplished by filtering and downsampling the quantizer output, thus the output stage of a Σ-Δ ADC consists of digital filters and a decimation process [68].

The discrete-time linear block $P(z)$ of the model (see figure 6.1) consists of a cascade



(a) Linear fit (b) Polynomial fit

Figure 6.9: Least squares fitting residuals in (μV/V) relative to 1 V for a k=2 (95 %) prediction interval. (a) Linear fit, (b) Polynomial fit. Equivalent sampling rate 16 kHz



(a) Linear fit (b) Polynomial fit

Figure 6.10: Least squares fitting residuals in (μV/V) relative to 1 V for a k=2 (95 %) prediction interval. (a) Linear fit, (b) Polynomial fit. Equivalent sampling rate 8 kHz

of three decimation filters as has been introduced in section 2.3.6. Figure 6.12 illustrates the decimation filters structure in detail.

These three filters decimate or downsample the output signal of the Σ-Δ modulator by a total factor M_T equal to

$$M_T = M_1 \cdot M_2 \cdot M_3\,, \tag{6.4}$$

where M_i is the decimation factor of stage i. The decimation factors are $M_1 = 4$, $M_2 = 32$ and $M_3 = 2$ given a total decimation factor $M_T = 256$.

The overall transfer function $P(z)$ related to the equivalent sampling rate at the filters

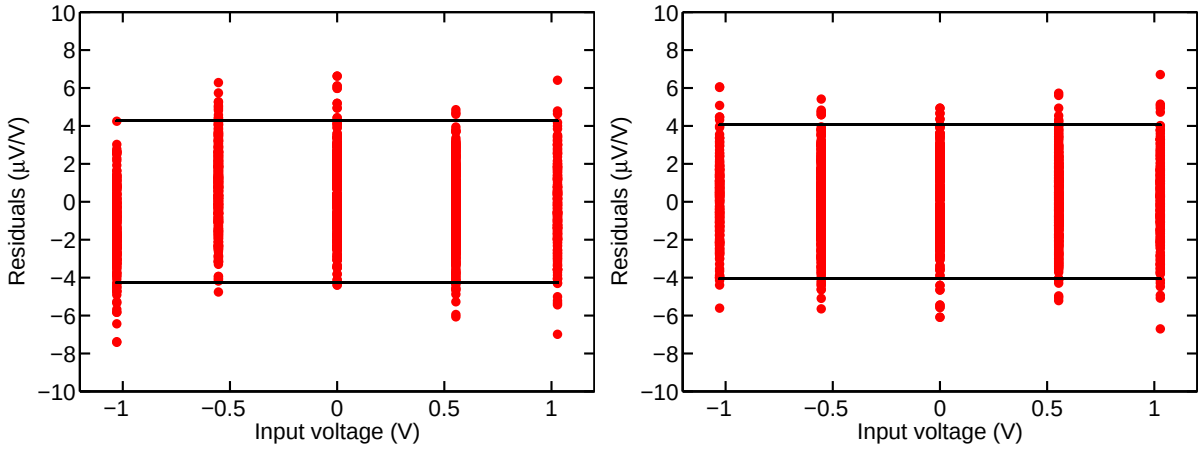


Figure 6.11: Least squares fitting residuals in (μV/V) relative to 1 V for a k=2 (95 %) prediction interval. (a) Linear fit, (b) Polynomial fit. Equivalent sampling rate 4 kHz

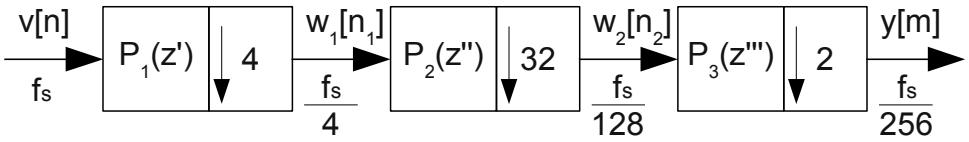


Figure 6.12: Block diagram of the decimation filters

output is given by

$$P(z) = P_1(z^{'}) \cdot P_2(z^{''}) \cdot P_3(z^{'''}), \tag{6.5}$$

where $P_i(z)$ is the transfer function of each filter stage. Replacing $z = e^{j2\pi f/(f_s/256)}$, the overall frequency response can be calculated and its magnitude ($|P(e^{j2\pi f/(f_s/256)})|$) (i.e. gain) is depicted in figure 6.13.

From figure 6.13 it is possible to see the ripple in the pass-band and the cut-off frequency of the overall frequency response of the decimation filters. The normalized cut-off frequency is ≈ 0.4 which reduces the bandwidth of the system to ≈ 0.4 of the Nyquist rate.

When sampling a signal the amplitude and phase are modified by the frequency response of the decimation filters, therefore the ADC readout must be corrected. The post-compensation is the inverse of the overall frequency response $P(z)$, normalized to the frequency response P_0 at DC. Hence, for an input signal frequency f and a sampling rate f_s, the correction factor $K_D(f, f_s)$ in the frequency domain is calculated using the expression

$$K_D(f, f_s) = P(e^{j2\pi f/(f_s/256)}) \cdot P_0, \tag{6.6}$$

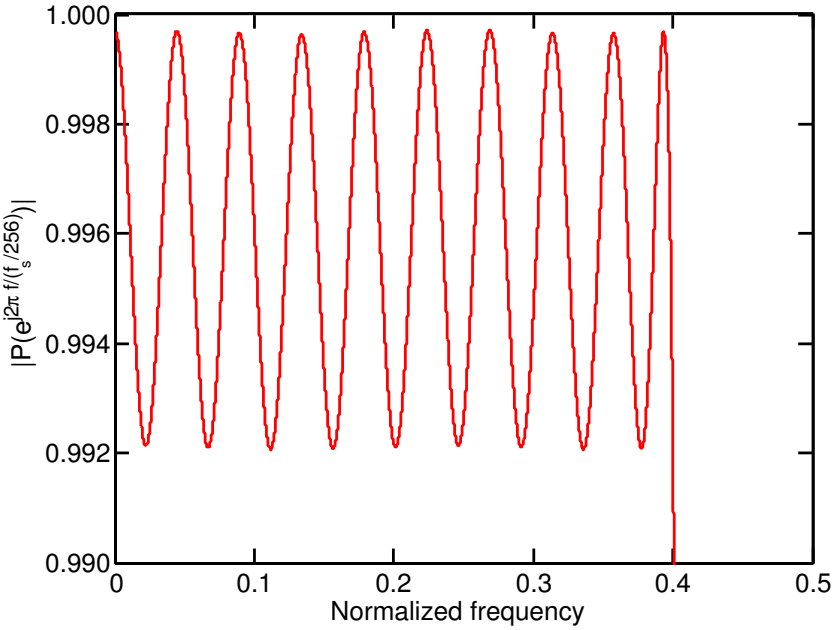


Figure 6.13: Magnitude of the overall frequency response of the decimation filters $|P(e^{j\omega})|$ normalized to $\frac{f}{f_s}256$

where P_0 is equal to the product of the sum of the filters coefficients, which is given by

$$P_0 = \sum_{n=1}^{N_1} p_1(n) \cdot \sum_{n=1}^{N_2} p_2(n) \cdot \sum_{n=1}^{N_3} p_3(n)\,, \tag{6.7}$$

where $p_i(n)$ are the coefficients of the filter i and N_1, N_2, N_3 are the lengths of the filters. As has been described in section 4.4.2 these filters are linear phase [69], thus the input signal is only delayed in time, therefore a compensation for phase distortion is not needed to apply. As a result, the compensation ($K_D(f, f_s)$) is the inverse of the magnitude (gain deviation) of the frequency response of the decimation filters.

6.3.1 Complete Transfer Function of the Model

In the foregoing section the Hammerstein model has been identified. Then, the post-compensation functions have been obtained. A fourth order polynomial $r(\cdot)$ to compensate the ADC readouts for non-linearities, analogue electronics gain and offset deviations. And, the post-compensation $K_D(f, f_s)$ for the decimation filter frequency response has been described. With these functions it is possible to express the reconstruction process of the input signal to the sampling system in terms of an inverse transfer function TF as

$$TF(y[m], f, f_s) = r(y[m], f_s) \cdot K_D(f, f_s)\,, \tag{6.8}$$

where $y[m]$ are the ADC readouts, f is the input signal frequency and f_s is the equivalent sampling rate.

6.4 Additional Compensations

The input signal applied to the system is also affected by the frequency response of the anti-aliasing filter and for the transfer function of ADC front-end zero-order hold. As a consequence, two additional compensations have to be applied to the sampled data: i) compensation for the fully differential amplifier anti-aliasing filters and ii) compensation for the zero-order hold of the sampling process.

6.4.1 Compensation for the Fully Differential Amplifier Anti-aliasing Filter

As it has been described in section 3.1.2 the FDA was configured as a second order anti-aliasing filter (see figure 3.4) with poles at $f_{p1} = 1/(2\pi R_f C_f)$ and $f_{p2} = 1/(2\pi R_s 2C_s)$. The transfer function $G(f)$ is

$$G(f) = G_0 \cdot \frac{1}{(1 + j2\pi f R_f C_f)} \cdot \frac{1}{(1 + j2\pi f R_s 2C_s)}\,, \tag{6.9}$$

where G_0 is the gain at DC ($f = 0$). This transfer function attenuates the amplitude of the input signal, thus a correction K_{FDA} must be applied on the sampled data. This correction depends on the input signal frequency f and is calculated using the following expression

$$K_{FDA}(f) = \sqrt{1 + \left(\frac{f}{f_{p1}}\right)^2} \cdot \sqrt{1 + \left(\frac{f}{f_{p2}}\right)^2}\,, \tag{6.10}$$

where $f_{p1} = 1/(2\pi R_f C_f)$ and $f_{p2} = 1/(2\pi R_s 2C_s)$ are the cut-off frequency of the FDA low-pass filters. Figure 6.14 illustrates the magnitude of the correction in the frequency range from DC to 5 kHz. As can be seen from figure 6.14 the correction stays below $1 \cdot 10^{-6}$ in the frequency range up to 500 Hz and increases from $3 \cdot 10^{-6}$ to $12.92 \cdot 10^{-6}$ in the range from 1 kHz to 2 kHz.

6.4.2 Zero-Order Hold Compensation

The AD7763 Σ-Δ ADC employs a double sampling technique front end. With this technique the ADC works at both phases of the internal clock and samples the input signal twice. As a result, the sampling rate is doubled without doubling the speed of the

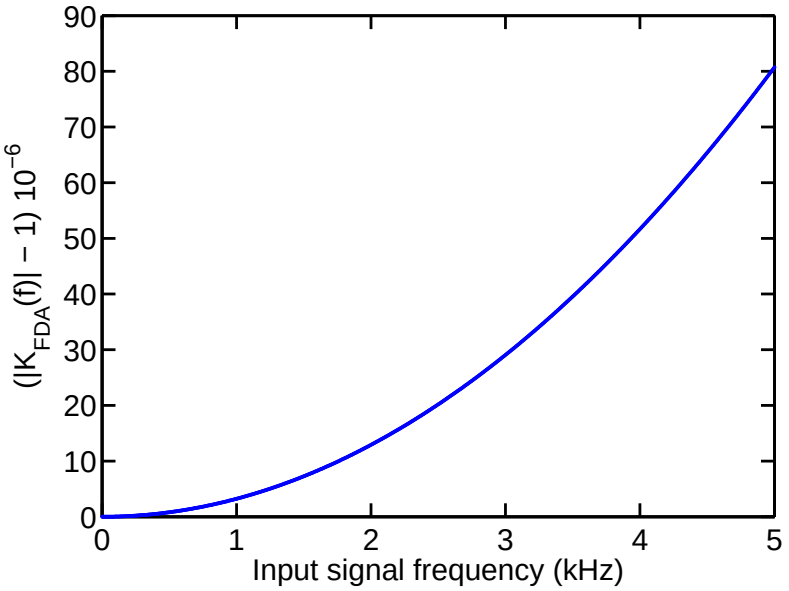


Figure 6.14: FDA anti-aliasing filters frequency response compensation. The correction at the maximum frequency of interest (f=2kHz) is $12.92 \cdot 10^{-6}$

ADC internal circuitry [92, 93].

A simplified block diagram of the ADC input stage is illustrated in figure 6.15 [27]. The sampling switches SS_1 and SS_3 are driven by ϕ_1, during the active pulse the input signal is connected to Cs_1. SS_1 and SS_3 are opened on the falling edge of ϕ_1 while SH_1 and SH_3 are closed, connecting Cs_1 to the Σ-Δ modulator. Likewise, switches SS_2, SS_4 are driven by ϕ_2, the input signal is connected to Cs_2 on the active pulse of ϕ_2. On the rising edge of ϕ_2, SS_2 and SS_4 are opened and Cs_2 is connected to the Σ-Δ modulator by SH_2 and SH_4. As a result, the input signal is sampled during a time equal to $T_s/4$ ($T_s = 1/f_s$ sampling time).

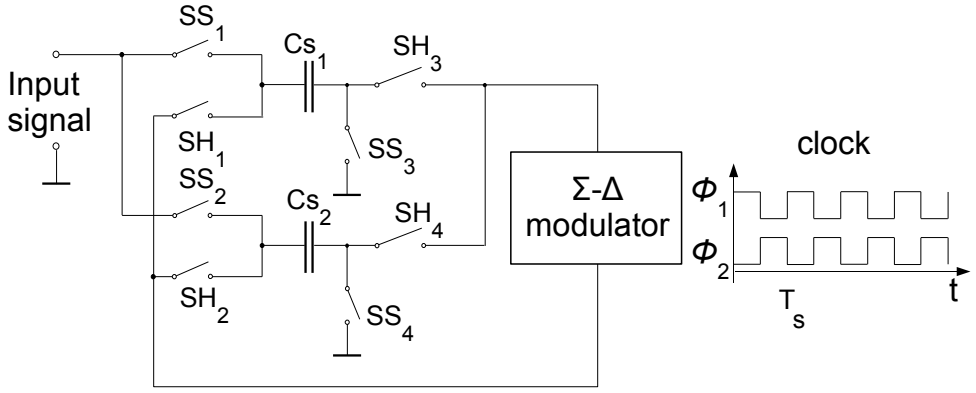


Figure 6.15: Simplified diagram of the ADC input front end from reference [27]

This front end can be modeled as a zero-order hold (ZOH) system [94] as depicted in figure 6.16. The output of a zero-order hold, with sampling time T_s takes the value of the

input $x(t)$ at a given instant t and remains constant until $t + T_s$, when it instantaneously changes to $x(t + T_s)$.

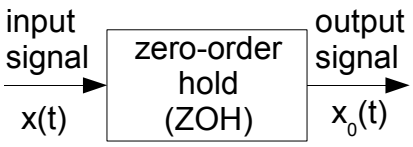


Figure 6.16: Zero-order hold model

The transfer function in the frequency domain $H_{ZOH}(f, T_s)$ of the zero-order hold is given by

$$H_{ZOH}(f, T_s) = \frac{\sin(2\,\pi f T_s/4)}{(2\,\pi f T_s/4)}\, e^{-j2\pi f T_s/4} = \frac{\sin(\pi f T_s/2)}{(\pi f T_s/2)}\, e^{-j\pi f T_s/2}\,, \tag{6.11}$$

where f is the frequency of the input signal. The output signal $x_0(t)$ can be compensated for the effect of the zero-order hold by a low-pass filter with frequency response equal to the inverse of $H_{ZOH}(f, T_s)$, $Hr_{ZOH}(f, T_s)$

$$Hr_{ZOH}(f, T_s) = \frac{1}{H_{ZOH}(f, T_s)} = \frac{(\pi f T_s/2)}{\sin(\pi f T_s/2)}\, e^{j\pi f T_s/2}\,. \tag{6.12}$$

Replacing T_s by its reciprocal, the sampling frequency f_s, equation (6.12) becomes

$$Hr_{ZOH}(f, f_s) = \frac{1}{H_{ZOH}(f, f_s)} = \frac{(\pi f/(2f_s))}{\sin(\pi f/(2f_s))}\, e^{j\pi f/(2f_s)}\,. \tag{6.13}$$

The compensation for the ZOH is the magnitude of $Hr_{ZOH}(f, f_s)$,

$$K_{ZOH}(f, f_s) = |Hr_{ZOH}(f, f_s)| = \left|\frac{(\pi\, f/(2f_s))}{\sin(\pi\, f/(2f_s))}\right|\,. \tag{6.14}$$

The correction $K_{ZOH}(f, f_s)$ (deviation from 1) is shown in figure 6.17 for sampling rates from 1024 kHz to 16384 kHz. On this figure, it can be observed that the correction to apply to the ADC readouts are below $0.5 \cdot 10^{-6}$ for the sampling rates $f_s = 16384$ kHz, $f_s = 8192$ kHz and $f_s = 4096$ kHz over the frequency range of interest. And, the correction becomes significant as the sampling rate reduces and the input signal frequency increases. In the frequency range below 2 kHz, the compensation stays below $0.5{\cdot}10^{-6}$ when sampling at 2048 kHz, but rises to $1.5 \cdot 10^{-6}$ for $f_s = 1024$ kHz.

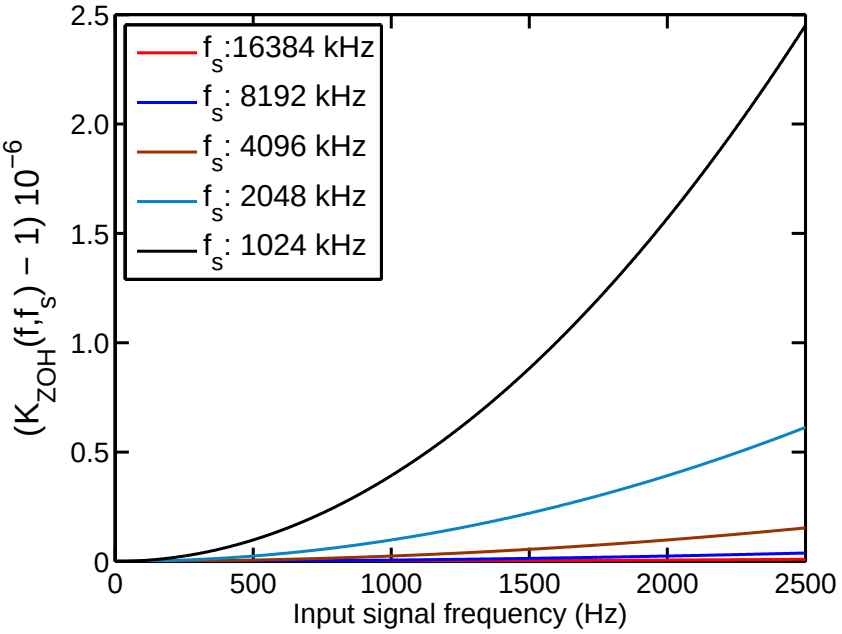


Figure 6.17: Compensation for the zero-order hold

6.5 Complete Sampling System Mathematical Model

Using all these building blocks, the M_T-downsampled reconstructed input signal $\tilde{x}[nM_T]$ can be calculated from the readouts of the ADC. The signal $\tilde{x}[nM_T]$ which reconstructs the M_T-downsampled $x[nM_T]$ is then obtained by the following expression

$$\begin{aligned} \tilde{x}[nM_T] = \tilde{x}[m] &= \underbrace{r(y[m], f_s) \cdot K_D(f_0, f_s)}_{\text{Hammerstein model}} \cdot K_{FDA}(f_0) \cdot K_{ZOH}(f_0, f_s) \\ &= TF\left(y[m], f_0, f_s\right) \cdot K_{FDA}(f_0) \cdot K_{ZOH}(f_0, f_s)\,, \end{aligned} \tag{6.15}$$

where $y[m]$ are the system readouts, f_0 is the input signal frequency and f_s is the equivalent sampling rate. $TF\left(y[m], f_0, f_s\right)$ is given by equation (6.8), $K_{FDA}(f_0)$ (see equation (6.10)) is the gain compensation for the anti-aliasing filter at frequency f_0 and $K_{ZOH}(f_0, f_s)$, which is given by equation (6.14), is the gain compensation for the zero-order hold at frequency f_0.

6.5.1 Model Extension to Multi-Frequency Input Signals

The mathematical model of the system given by equation (6.15) can be applied to input signals with one fundamental frequency component f_0. In the case of input signals with

two or more frequency components described as

$$x(t) = \sum_{k=0}^{K-1} A_k \, \sin\left(2\,\pi\, f_k t\right) \,, \tag{6.16}$$

where K is the number of frequencies, A_k is the amplitude and f_k is the frequency of the component k, the model has to be extended. This input signal is sampled at a sampling rate f_s by the system and the output $y[m]$ is

$$y[m] = \sum_{k=0}^{K-1} A_k \, \sin\left[2\,\pi\, f_k/f_s m\right] \,. \tag{6.17}$$

To obtain the downsampled reconstructed input signal $\tilde{x}[nM_T]$ as in equation (6.15) the corrections K_D, K_{FDA} and K_{ZOH} which are frequency dependent must to be applied to all frequency components present on the output signal $y[m]$, this can be performed in the frequency domain. As a consequence, the reconstruction equation (6.15) becomes

$$\tilde{X}(f_k) = W(f_k) \cdot K_D(f_k, f_s) \cdot K_{FDA}(f_k) \cdot K_{ZOH}(f_k, f_s) \quad k = 0, \ldots, K-1 \,, \tag{6.18}$$

where $\tilde{X}(f_k)$ is the discrete Fourier transform [69] of $\tilde{x}[m]$ and $W(f_k)$ is the discrete Fourier transform of output $w[m] = r(y[m], f_s)$ of the reconstruction polynomial $r(\cdot)$.

6.6 Uncertainty Evaluation

The readouts of the sampling system are affected by deviations from the different modules of the sampling system. To correct the readouts in order to reconstruct the input signal a number of corrections must be applied. These corrections are known up to a certain level, because they are constructed from observed data. Therefore a mathematical model is built and used to evaluate the total uncertainty of the reconstructed signal.

6.6.1 Mathematical Model for Uncertainty Evaluation

The post-compensating model, the anti-aliasing filter compensation and zero-order hold compensation have been analyzed and described in previous sections. In addition, a Type-A uncertainty contribution for the model has been described in section 4.5. A complete uncertainty evaluation is presented here.

The reconstructed signal $\tilde{x}[nM_T]$ is given by equation (6.15). Each of the building blocks in the model used to reconstruct the signal introduces an uncertainty to the final result. Applying the uncertainty propagation law, without correlation, the combined

standard uncertainty $u_c(\tilde{x})$ of the measurand $\tilde{x}$ is the square root of the estimated variance $u_c^2(\tilde{x})$ [56], which is obtained from

$$u_c^2(\tilde{x}) = \left(\frac{\partial \tilde{x}}{\partial TF}\right)^2 u^2(TF) + \left(\frac{\partial \tilde{x}}{\partial K_{FDA}}\right)^2 u^2(K_{FDA}) + \left(\frac{\partial \tilde{x}}{\partial K_{ZOH}}\right)^2 u^2(K_{ZOH})\,. \quad (6.19)$$

Where

$$\begin{aligned} c_1 &= \frac{\partial \tilde{x}}{\partial TF} = K_{FDA}(f) \cdot K_{ZOH}(f, f_s) \\ c_2 &= \frac{\partial \tilde{x}}{\partial K_{FDA}} = TF\left(y[m], f, f_s\right) \cdot K_{ZOH}(f, f_s) \\ c_3 &= \frac{\partial \tilde{x}}{\partial K_{ZOH}} = TF\left(y[m], f, f_s\right) \cdot K_{FDA}(f)\,, \end{aligned}$$

are the sensitivity coefficients.

The total uncertainty $u(TF)$ is the combination of the uncertainty of the prediction interval of a new value using the post-compensation Hammerstein model, the system resolution and the voltage reference variation because of changing the sampling rate during measurements (see section 3.2.3). This is the main uncertainty source to the final value, which is in the interval from 2 μV/V at an equivalent sampling rate of 4 kHz to 30 μV/V at an equivalent sampling rate of 64 kHz.

The uncertainty $u(K_{FDA})$ corresponds to the indeterminate value of the cut-off frequency of the low-pass filter. The main contribution to this uncertainty comes from the mismatch of the electronic components (the estimation of this uncertainty is described in appendix A).

While the uncertainty $u(K_{ZOH})$ is due to the indeterminate value of the sampling time T_s, the main contribution it is derived from the accuracy of the reference clock (internal or external) which supplies the system with the sampling clock. Using an internal clock with an accuracy of 100 μHz/Hz, the maximum uncertainty contribution to the uncertainty of $\tilde{x}$ is $\approx 0.2 \cdot 10^{-3} \mu$V/V in the frequency band of interest, thus this contribution can be neglected in comparison with the contribution of $u(TF)$ and $u(K_{FDA})$. The calculation of $u(K_{ZOH})$ is summarized in appendix A.

6.7 Calculation of the Root-mean-square Value

In the foregoing sections the complete model of the sampling system has been obtained. As validation procedure of the model the root-mean-square (rms) value of a periodic signal, i.e. a sinusoidal signal, has been calculated. The experimental validation of the model is presented in chapter 7, here a procedure to compute the rms value from the

sampled data in the time domain and in the frequency domain is described.

The rms value of a periodic signal may be computed in the time domain or in the frequency domain. For the case of a continuous-time sinusoidal signal $x_c(t)$ with amplitude A_0, fundamental frequency $f_0 = 1/T_0$ (T_0 the fundamental period) and initial phase ϕ modeled as

$$x_c(t) = A_0 \sin(2\,\pi\,f_0\,t + \phi)\,. \tag{6.20}$$

The rms value of $x_c(t)$, in the time domain, is given by the following expression

$$V_{rms} = \sqrt{\frac{1}{T_0}\int_0^{T_0} \left(A_0\,\sin(2\,\pi\,f_0\,t + \phi)\right)^2\,dt}\,. \tag{6.21}$$

A discrete-time signal $x(nT_s)$ can be obtained by sampling $x_c(t)$ at a sampling rate $T_s = 1/f_s$, hence assuming ideal sampling

$$x(nT_s) = A_0 \sin(2\,\pi\,f_0\,n\,T_s + \phi) \qquad n = 0, 1, \ldots, N-1\,, \tag{6.22}$$

where N is the total number of samples acquired. Then, the rms value of one period of the sampled signal $x(nT_s)$ can be calculated using the following expression

$$V_{rms} = \sqrt{\frac{1}{N_p}\sum_{n=0}^{(N_p-1)} \left(A_0\,\sin(2\,\pi\,f_0\,n\,T_s + \phi)\right)^2}\,, \tag{6.23}$$

where N_p is the number of samples per period. Expanding the summation of equation (6.23), it results in

$$\begin{aligned} V_{rms} &= \sqrt{\frac{A_0^2}{2} - \frac{A_0^2}{2}\,\frac{\sin\left(4\,\pi\,f_0\,N_p\,T_s + 2\phi\right)}{\left(4\,\pi\,f_0\,N_p\,T_s\right)} + \frac{A_0^2}{2}\,\frac{\sin(2\phi)}{\left(4\,\pi\,f_0\,N_p\,T_s\right)}} \\ &= \sqrt{\frac{A_0^2}{2}\left(1 - \frac{\sin\left(4\,\pi\,f_0\,N_p\,T_s + 2\phi\right)}{\left(4\,\pi\,f_0\,N_p\,T_s\right)} + \frac{\sin(2\phi)}{\left(4\,\pi\,f_0\,N_p\,T_s\right)}\right)}\,, \end{aligned} \tag{6.24}$$

If the conditions of ideal and coherent sampling are fulfilled, that is $T_0/T_s = J$ with J an integer number, thus equation (6.24) reduces to

$$V_{rms} = \frac{A_0}{\sqrt{2}}\,. \tag{6.25}$$

Similarly, in the frequency domain, the rms value is obtained by computing the discrete Fourier transform (DFT) on the sampled signal $x(nT_s)$. The DFT of $x(nT_s)$ is

defined as

$$X(f_k) = \sum_{n=0}^{N-1} x(nT_s) e^{-j\,2\,\pi\,f_k\,n\,T_s}\,, \tag{6.26}$$

with

$$f_k = 0,\, 1/(NT_s),\, 2/(NT_s),\, \cdots,\, (N-1)/(NT_s)\,,$$

and N the total number of samples.

The amplitude of the k^{th} harmonic is given by $2|X(f_k)]/N$, considering only positive frequencies. Thus, for the sinusoidal signal $x(nT_s)$, the DFT is a pair of impulses at frequencies $-f_0$ and f_0 with amplitude equal to $-A_0/2$ and $A_0/2$, respectively, provided ideal and coherent sampling.

Hence, the rms value V_{rms} of $x(nT_s)$ is equal to

$$V_{rms} = \frac{\sqrt{2}}{N}\,|X(f_0)| = \frac{A_0}{\sqrt{2}}\,. \tag{6.27}$$

The frequency method is often preferred because it gives information regarding the harmonic components present in the signal.

When sampling a signal using a real ADC, it introduces additional errors, i.e. noise, resolution, gain error and non-linearities, thus an additional term has to be included in equations (6.25) and (6.27). If the conditions of coherent sampling are fulfilled ($T_0/T_s = J$ with J an integer number) the rms value becomes

$$V_{rms} = \frac{A_0}{\sqrt{2}} + \epsilon\,. \tag{6.28}$$

where ϵ represents deviations introduced by the sampling system.

Equation (6.27) can be extended when measuring multi-frequency signals, harmonically related or not. Modeling the multi-frequency signal as

$$x_m(nT_s) = \sum_{k=0}^{K-1} A_k\, \sin\left(2\,\pi\,f_k n T_s\right) \quad n = 0, 1, \ldots, N-1\,, \tag{6.29}$$

where N is the total number of samples, K is the number of frequencies, A_k is the amplitude and f_k is the frequency of the frequency component k, respectively. The DFT $X_m(f_k)$ of the signal $x_m(nT_s)$ is calculated using equation (6.26), then the rms value, considering only positive frequencies, of each frequency component k is given by

$$V_{rms_k}(f_k) = \frac{\sqrt{2}}{N}\,|X_m(f_k)| \tag{6.30}$$

provided the number of samples acquired N encompasses integer number of periods of all frequency components in the signal. Otherwise, windowing is necessary to minimize the error due to spectral leakage [95].

In addition, the total rms value of the signal can be obtained by the Parseval's theorem [69] which states that

$$\sum_{n=0}^{N-1} |x_m(nT_s)|^2 = \frac{1}{N} \sum_{k=0}^{N-1} |X_m(f_k)|^2 \,, \tag{6.31}$$

where N is the total number of samples. From the Parseval's theorem follows

$$V_{rms_T} = \frac{1}{N} \sqrt{\sum_{k=0}^{N-1} |X_m(f_k)|^2} \,. \tag{6.32}$$

Equation (6.32) extends the computation of the rms value to arbitrary signals.

6.7.1 Compensation for the Finite Number of Samples per Period

In a sampling system, the discrete-time signal is a replica of the continuous-time signal with a finite number of samples. In addition, the Σ-Δ ADC decimates or downsamples its input signal by an integer decimation factor M_T.

For a signal $x(nT_s)$ described by equation (6.22) the samples are uniformly distributed over the signal periods. The distance in time between samples is the sampling time T_s, or in number of samples, in one period is $2\pi/N_p$, where N_p is the number of samples per period.

When computing the rms value of the signal the voltage value between sample iT_s and sample $(i+1)T_s$ is assumed constant and equal to the voltage value of the sample $x(iT_s)$. This process can be described as performing the convolution of the discrete-time signal $x(nT_s)$ with a rectangular pulse signal with duration $T_{rect} = (i+1)T_s - iT_s = T_s$ as described by

$$x_r(nT_s) = \sum_{k=0}^{N_p-1} x(kT_s)\, h_{rect}(nT_s - kT_s) \,, \tag{6.33}$$

where

$$h_{rect}(nT_s) = \begin{cases} 1 & nT_s \leq (n+1)T_s, \\ 0 & \text{otherwise.} \end{cases} \tag{6.34}$$

The frequency response of $h_{rect}(nT_s)$ is

$$H_{rect}(f) = \frac{\sin(\pi\, f\, T_s)}{\pi\, f\, T_s} e^{-j\,\pi\, f\, T_s} \,, \tag{6.35}$$

where T_s is the sampling time at the Σ-Δ ADC front-end. This frequency response is known as the *sinc function* ($sinc(x) = \sin(x)/x$). This procedure is similar to what is called in the literature as zero-order interpolation of a discrete-time signal [68, 69]. In this procedure $x(nT_s)$ is filtered by a low-pass filter with frequency response given by equation (6.35) to reconstruct the input signal. Thus, after the reconstruction the output signal of this filter has to be compensated by the attenuation produced by the frequency response of the filter to the signal $x(nT_s)$. Therefore, the signal $x_r(nT_s)$ is then compensated by $[H_{rect}(f)]^{-1}$, this compensation is known as compensation for zero-order hold interpolator [69].

The Σ-Δ ADC sampled a time domain signal present at its input at a sampling rate equal to f_s, then the signal is downsampled by the decimation filters, as has been described in section 6.3. As a result, the signal is downsampled 4 times by the first decimation stage, 32 times by the second decimation stage and 2 times by the third decimation stage, as a result the equivalent sampling rate is equal to $f_{seq} = f_s/256$. Hence, the correction $K_{sinc}(f_0, f_s)$ to apply is given by

$$K_{sinc}(f_0, f_s) = K_{sinc_1}(f_0, f_s) \cdot K_{sinc_2}(f_0, f_s) \cdot K_{sinc_3}(f_0, f_s)\,, \tag{6.36}$$

with

$$K_{sinc_i}(f_0, f_s) = \frac{\pi f_0 f_s^{-1} M_i}{\sin(\pi f_0 f_s^{-1} M_i)}$$

where f_0 is the input signal fundamental frequency, f_s is the Σ-Δ modulator sampling rate and M_i (with $i = 1, 2, 3$) is the decimation factor of stage i, i.e. $M_1 = 4$, $M_2 = 32$ and $M_3 = 2$. Then the rms value given by equation (6.27) becomes

$$V_{rms} = \frac{\sqrt{2}}{N} \left|X_0(f_0)\right| \cdot K_{sinc}(f_0, f_s)\,, \tag{6.37}$$

with X_0 the DFT of $x(nT_s)$, N the total number of samples and f_0 the fundamental frequency.

Equation (6.37) can be extended to correct the rms value of each frequency component in a multi-frequency signal. Thus, assuming an input signal $x_m(nT_s)$ described by equation (6.29) with $k = 0, \ldots, K-1$ frequencies, the rms value $V_{rms_k}(f_k)$ of each frequency f_k is

$$V_{rms_k}(f_k) = \frac{\sqrt{2}}{N} \left|X_m(f_k)\right| \cdot K_{sinc}(f_k, f_s) \quad k = 0, \ldots, K-1\,, \tag{6.38}$$

With this equation all frequency components in the input signal are compensated for the frequency response of h_{rect}.

Chapter 7

Experimental Validation of the Model

In previous chapters, the Σ-Δ sampling system post-compensating model and characterization have been described. This chapter adds the experimental validation of the model and the performance of the designed Σ-Δ sampling system when measuring an alternating signal.

7.1 Model Validation

Once the post-compensating model is determined its validation follows in order to evaluate the overall performance of the Σ-Δ sampling system. Model validation is a procedure to answer the question *whether for the application the model is good enough or not.* The validation procedure performed in this thesis was based on comparing measurement results with a high accuracy digital voltmeter, the Agilent model 3458A [84] under sinusoidal excitation. The input signal frequency range was from 62.5 Hz to 2 kHz with amplitude in the ≈ 1 V range. Many techniques were studied and developed for such purpose (see reference [15] for instance).

7.1.1 Measurement Setup

Figure 7.1 illustrates the measurement setup. A signal source, the Fluke 5700A calibrator [96], was used to generate sinusoidal signals with a nominal amplitude equal to 0.708 V rms in a frequency range from 62.5 Hz to 2 kHz. The Σ-Δ sampling system and the digital voltmeter (DVM) were connected to the signal source output. To avoid spectral leakage when computing the discrete Fourier transform, the source, the sampling system and the DVM were synchronized employing as a main clock signal the 20 MHz internal clock of the DVM. The clock signal from the DVM was optically isolated, to avoid interference (opto in figure 7.1). This optocoupler supplies two output signals, the 20 MHz output

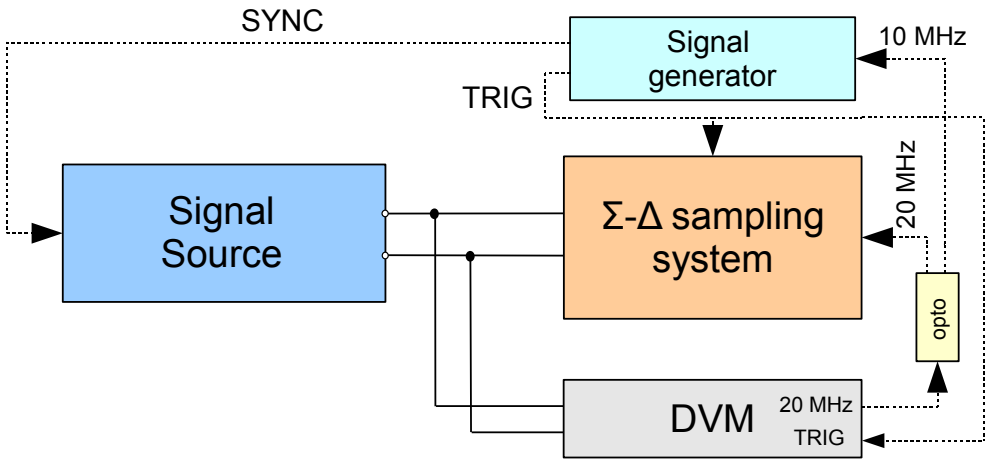


Figure 7.1: Measurement Setup

was connected to the Σ-Δ sampling system and the 10 MHz output was fed to a signal generator which was used to generate a SYNC signal to synchronize the signal source. In addition, the signal source triggered the DVM and the Σ-Δ sampling system.

7.1.2 Validation Results

A sinusoidal signal with nominal rms value equal to 0.708 V in the frequency range from 62.5 Hz to 2 kHz was acquired at different sampling rates, to validate the Σ-Δ sampling system model. At the same time, the DVM measured the same signal. The DVM was used as sampler, it was configured in DCV mode (DC voltage) and in the 10 V input range, the maximum input bandwidth in this mode is from DC to 150 kHz [84]. The sampling parameters for both systems are listed in table 7.1. These parameters were selected in order to fulfill the requirements of coherent sampling, so that the sampling rate was a multiple of the input signal frequency. As a result, spectral leakage when computing the discrete Fourier transform was avoided and an integer number of samples per period of the signal has been measured, in the case of the Σ-Δ sampling system the value M, as shown in fifth column of table 7.1. And, in the case of the DVM the number of samples per period was M = 16, for all cases but the last in which it was M = 8. The integration time T_{aper} was set equal to $T_s - 25\ \mu$s (T_s sampling time) to allow storing the measured samples in the DVM internal memory.

The total number of periods acquired have been split into different frames according to the observation time τ determined by the Allan deviation when characterizing the transfer function of the system (see section 6.2.2, table 6.2). Then, the rms value of each frame was calculated, in the frequency domain, using equation (6.27) and finally all rms values were averaged to obtain the final result.

The measurement results were divided in two groups: i) without applying the K_{sinc}

Table 7.1: Σ-Δ sampling system and DVM sampling configuration

f (Hz)	Σ-Δ				DVM				
	Eq. f_s (kHz)	Eq. T_s (μs)	BW (kHz)	M	f_s (kHz)	T_s (μs)	T_{aper} (μs)	BW (kHz)	M
62.5	4	250	2	64	1	1000	975	0.5	16
	8	125	4	128					
	16	62.5	8	256					
	32	31.25	16	512					
	64	15.625	32	1024					
125	4	250	2	32	2	500	475	1	16
	8	125	4	64					
	16	62.5	8	128					
	32	31.25	16	256					
	64	15.625	32	512					
250	4	250	2	16	4	250	225	2	16
	8	125	4	32					
	16	62.5	8	64					
	32	31.25	16	128					
	64	15.625	32	256					
500	8	125	4	16	8	125	100	4	16
	16	62.5	8	32					
	32	31.25	16	64					
	64	15.625	32	128					
1000	16	62.5	8	16	16	62.5	37.5	8	16
	32	31.25	16	32					
	64	15.625	32	64					
2000	32	31.25	16	16	16	62.5	37.5	8	8
	64	15.625	32	32					

correction and ii) with the K_{sinc} correction. The K_{sinc} is applied to the measured signal to compensate for the finite number of samples per period. For the Σ-Δ sampling system it has the form

$$K_{sinc} = \frac{(\pi f f_s^{-1})^3 M_1 M_2 M_3}{\sin(\pi f f_s^{-1} M_1)\sin(\pi f f_s^{-1} M_2)\sin(\pi f f_s^{-1} M_3)}\,, \tag{7.1}$$

where $M_1 = 4$, $M_2 = 32$ and $M_3 = 2$ are the decimation factors, f is the input signal fundamental frequency and f_s is the sampling frequency. In the case of the DVM the K_{sinc} correction is the transfer function of the integrating ADC (IADC) [43] and is given by

$$K_{sinc} = \frac{\pi f T_{aper}}{\sin(\pi f T_{aper})}\,, \tag{7.2}$$

where T_{aper} is the integration time.

The first group is shown in figures 7.2 to 7.7 and reported from tables 7.2 to 7.7. The dependence of V_{rms} with the equivalent sampling rate can be clearly observed.

The second group of results was obtained applying the K_{sinc} correction (see equations (6.37) and (7.1)) on the rms values of the first group. The results are shown from

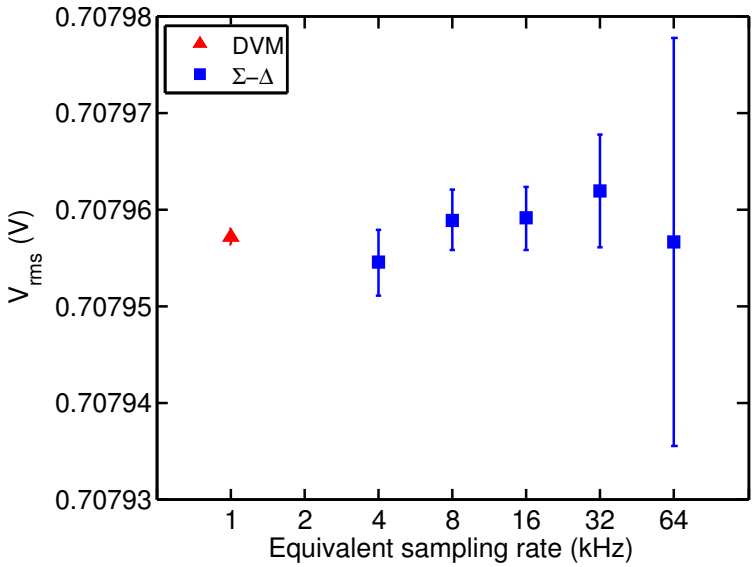


Figure 7.2: Input signal frequency 62.5 Hz

Table 7.2: Input signal frequency 62.5 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
4	0.7079546	3.4	4.8
8	0.7079590	3.2	4.5
16	0.7079592	3.2	4.5
32	0.7079620	5.9	8.3
64	0.7079568	21	29.7
DVM			
1	0.7079573	0.8	1.1

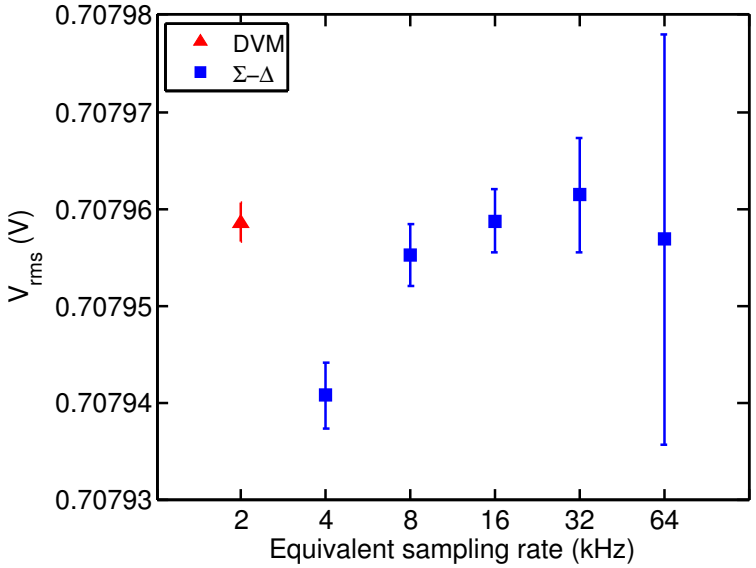


Figure 7.3: Input signal frequency 125 Hz

Table 7.3: Input signal frequency 125 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
4	0.7079409	3.4	4.8
8	0.7079553	3.2	4.5
16	0.7079588	3.2	4.5
32	0.7079615	5.9	8.3
64	0.7079569	21	29.7
DVM			
2	0.7079586	2.0	2.8

figure 7.8 to 7.13 and summarized from table 7.8 to 7.13. On the figures, the uncertainty bars indicate 1-σ (k=1). The K_{sinc} correction has compensated the rms values for the finite number of samples when the number of samples per period is 16 or higher. As a consequence, the corrected values are within the combined uncertainty of the DVM for a coverage factor k=2 (95 %). For lower number of samples per period, the settling time of the decimation filters affects the results as it will be explained below.

These results show that the designed sampling system is in agreement with the DVM and alternating signals quantities can be measured in the frequency range from 62.5 Hz to 2 kHz with a combined uncertainty u_c in the order of 8 μV/V at an equivalent sampling

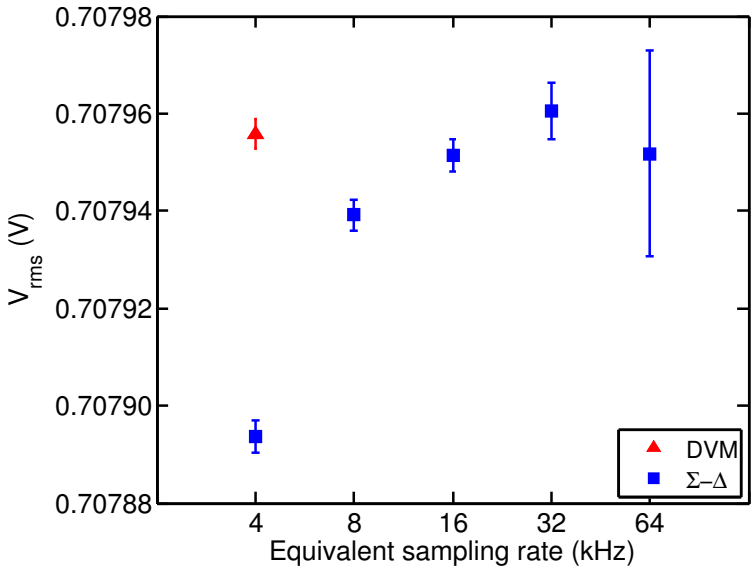


Figure 7.4: Input signal frequency 250 Hz

Table 7.4: Input signal frequency 250 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	$\left(\frac{\mu V}{V}\right)$
4	0.7078937	3.4	4.8
8	0.7079392	3.2	4.5
16	0.7079514	3.2	5.4
32	0.7079605	5.9	8.3
64	0.7079517	21	29.7
DVM			
4	0.7079559	3	4.2

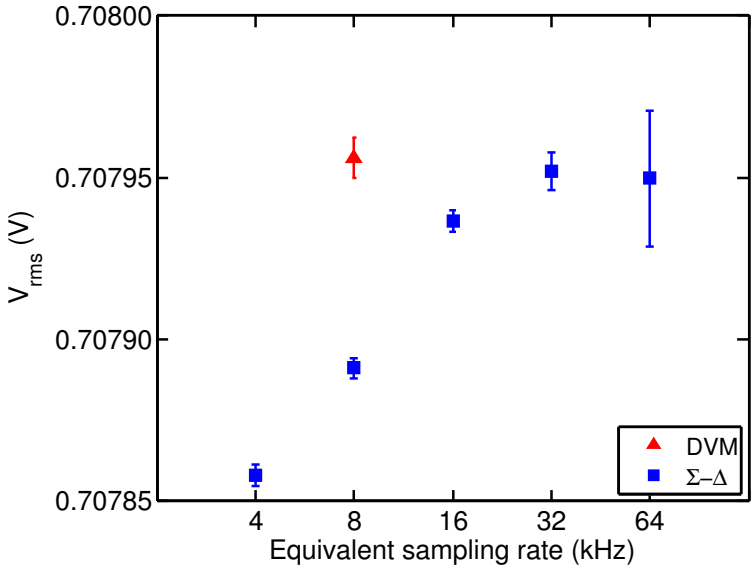


Figure 7.5: Input signal frequency 500 Hz

Table 7.5: Input signal frequency 500 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	$\left(\frac{\mu V}{V}\right)$
4	0.7078581	3.4	4.8
8	0.7078913	3.2	4.5
16	0.7079367	3.2	4.5
32	0.7079518	5.9	8.3
64	0.7079497	21	29.7
DVM			
8	0.7079563	6.2	8.8

rate of 32 kHz, under these measurement conditions. These results improve the uncertainty of the DVM which reaches 8 μV/V at 500 Hz. In addition, the effective bandwidth is also increased from 8 kHz of the DVM in DCV mode to 16 kHz of the Σ-Δ sampling system.

The validation results at 4 kHz sampling rate show that the rms value of an input signal in the frequency range from 62.5 Hz to 125 Hz can be measured with u_c=5 μV/V, with a bandwidth of 2 kHz. The effect of the decimation filters can be observed at 250 Hz where the rms value is slightly higher than the measured by the DVM, as can be seen in figure 7.10. Despite this, the rms values are within a coverage factor of 2-σ (k=2) .

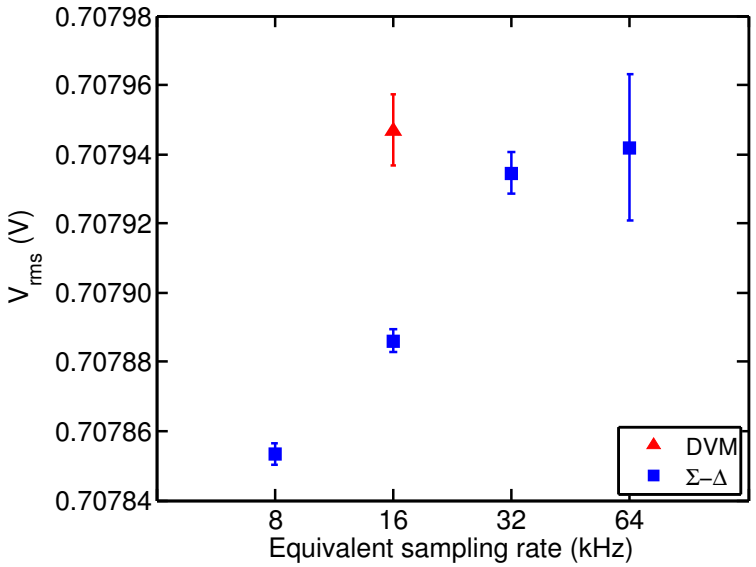


Figure 7.6: Input signal frequency 1 kHz

Table 7.6: Input signal frequency 1 kHz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
8	0.7078534	3.2	4.5
16	0.7078861	3.2	4.5
32	0.7079346	5.9	8.3
64	0.7079419	21	29.7
DVM			
16	0.7079473	10	14.1

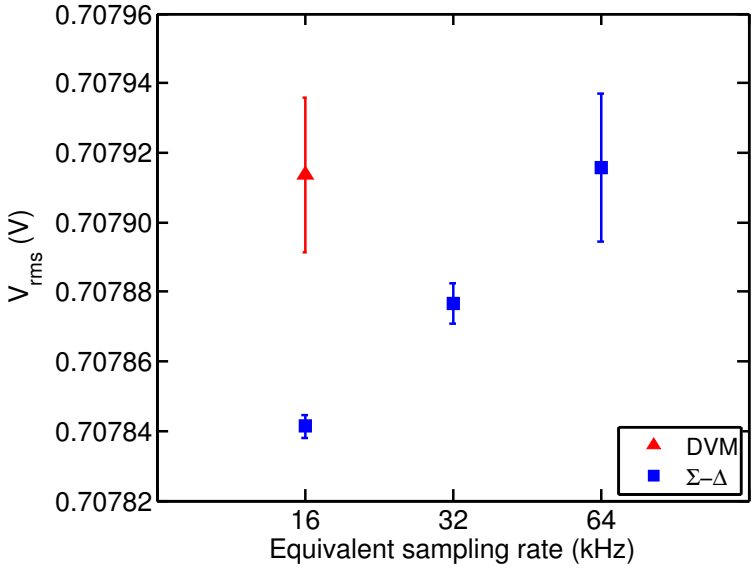


Figure 7.7: Input signal frequency 2 kHz

Table 7.7: Input signal frequency 2 kHz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
16	0.7078414	3.3	4.7
32	0.7078768	5.9	8.3
64	0.7079158	21	29.7
DVM			
16	0.7079136	22	31.1

When the sampling rate is equal to 8 kHz, the results show that the agreement within the uncertainty level of the DVM extends the input signal frequency range to 500 Hz with u_c=5 μV/V, in this case the bandwidth of the Σ-Δ sampling system is 4 kHz. Again, these results show an improvement. The DVM has a combined uncertainty equal to 8.8 μV/V with the same sampling rate, as it is reported in table 7.11.

As table 7.12 shows, with a sampling rate of 16 kHz the u_c of the Σ-Δ sampling system is also equal to 5 μV/V, and the DVM has an u_c=14 μV/V when the input signal frequency is 1 kHz.

At higher sampling rates, 32 kHz and 64 kHz, the combined uncertainties were 8 μV/V

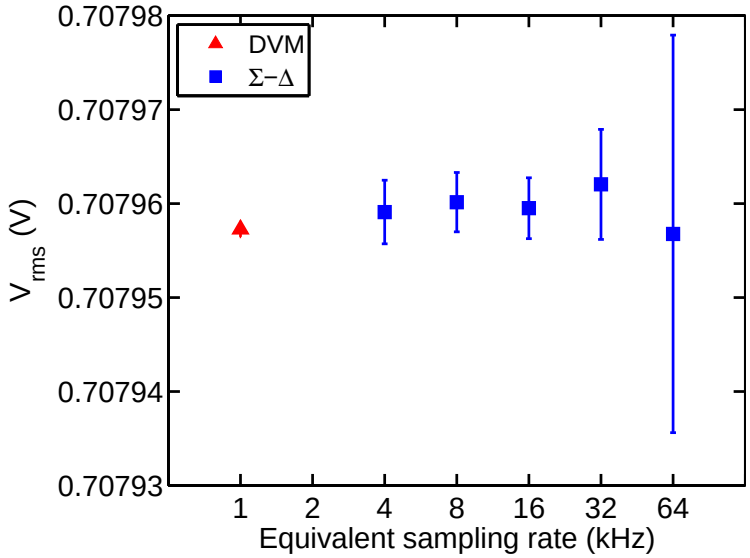


Figure 7.8: Input signal frequency 62.5 Hz

Table 7.8: Input signal frequency 62.5 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
4	0.7079591	3.4	4.8
8	0.7079602	3.2	4.5
16	0.7079595	3.2	4.5
32	0.7079620	5.9	8.3
64	0.7079568	21	29.7
DVM			
1	0.7079573	0.8	1.1

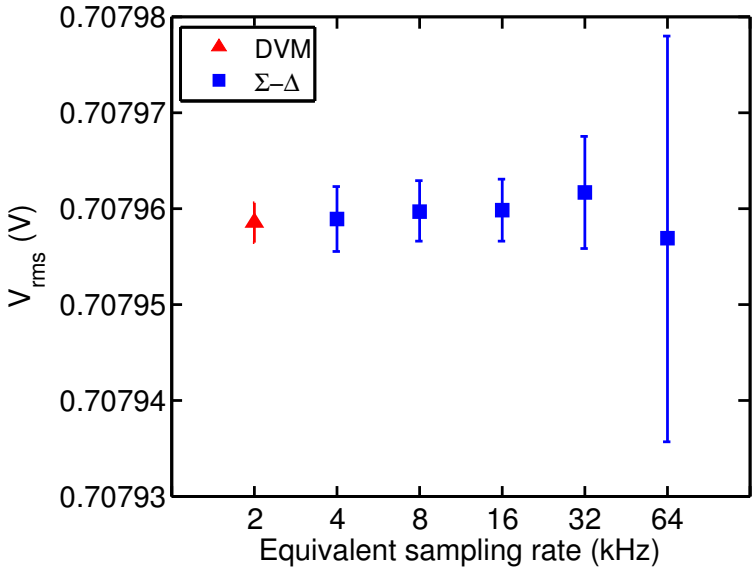


Figure 7.9: Input signal frequency 125 Hz

Table 7.9: Input signal frequency 125 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
4	0.7079589	3.4	4.8
8	0.7079598	3.2	4.5
16	0.7079599	3.2	4.5
32	0.7079617	5.9	8.3
64	0.7079570	21	29.7
DVM			
2	0.7079586	2	2.8

and 30 μV/V, respectively, over the total input signal frequency range from 62.5 Hz to 2 kHz. On this frequency range, the DVM increases its u_c to 31 μV/V. These results are summarized in table 7.13.

In the frequency range up to 100 Hz, the Σ-Δ sampling system has higher uncertainty than the DVM which has a combined uncertainty ≈1 μV/V.

As expected, the uncertainty increases with sampling rate because the non-linearities of the ADC are higher at high sampling rate as it has been reported in section 6.2.2 where the non-linear transfer function has been analyzed.

The dependence of the rms value with the number of samples per period deserves a

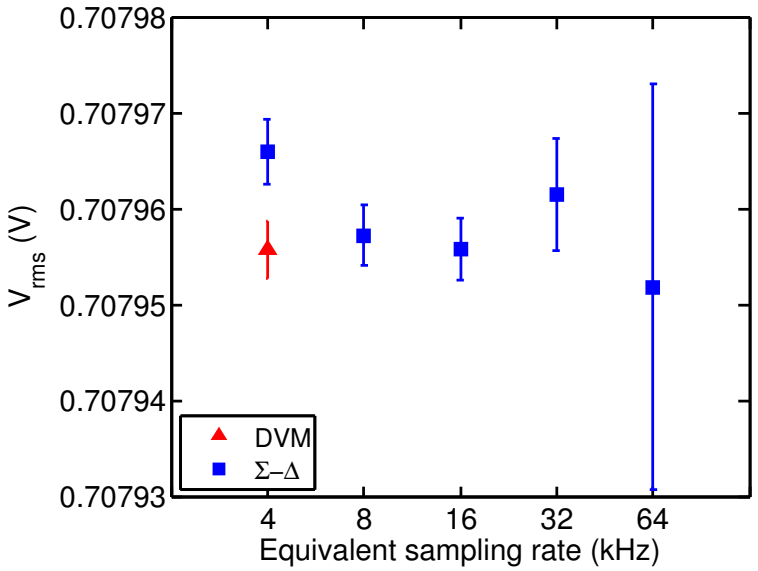


Figure 7.10: Input signal frequency 250 Hz

Table 7.10: Input signal frequency 250 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
4	0.7079661	3.4	4.8
8	0.7079573	3.2	4.5
16	0.7079559	3.2	4.5
32	0.7079616	5.9	8.3
64	0.7079520	21	29.7
DVM			
4	0.7079559	3	4.2

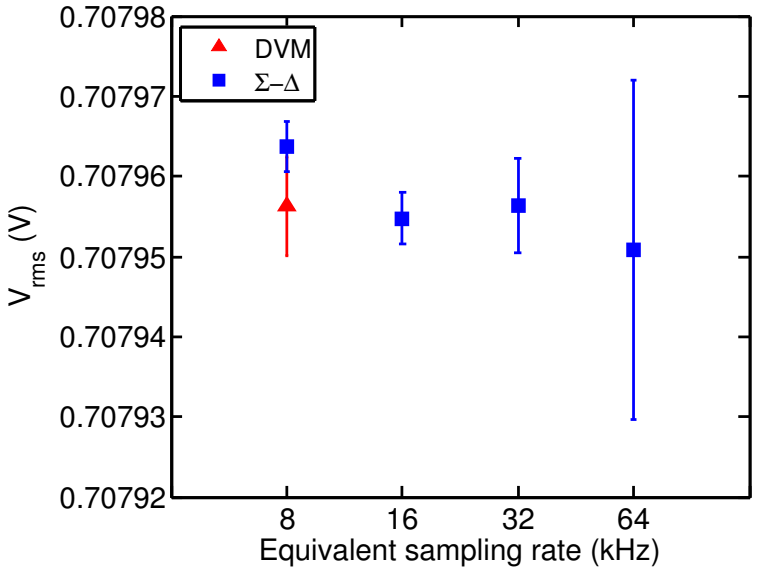


Figure 7.11: Input signal frequency 500 Hz

Table 7.11: Input signal frequency 500 Hz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	u_c $\left(\frac{\mu V}{V}\right)$
8	0.7079637	3.2	4.5
16	0.7079548	3.2	4.5
32	0.7079564	5.9	8.3
64	0.7079509	21	29.7
DVM			
8	0.7079563	6.2	8.8

special remark. The K_{sinc} correction must be applied to the readouts of any sampling system because of the finite sampling time. For the Σ-Δ ADC, apart from the sample-and-hold at the ADC front-end, the decimation filters are involved. The high rate output signal from the modulator is *averaged* by the decimation filters to obtain a high resolution lower rate readout [22]. As a consequence, the input signal at the ADC is *weighted* by the coefficients of the filters. If the number of samples in a period of the input signal is not sufficient the coefficients of the filters produce an additional error on the output readout which is proportional to the ratio between the input signal frequency and the sampling rate. To obtain high accuracy results the number of samples per period has to

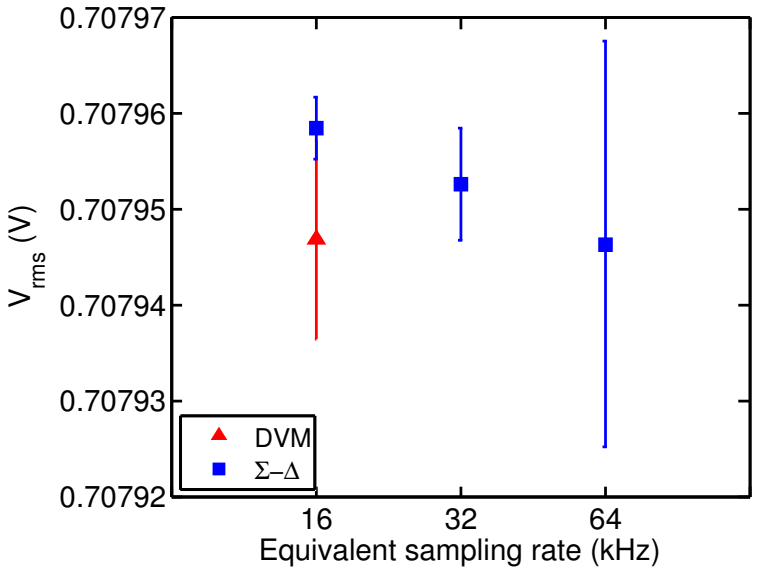


Figure 7.12: Input signal frequency 1 kHz

Table 7.12: Input signal frequency 1 kHz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	$\left(\frac{\mu V}{V}\right)$
16	0.7079585	3.3	4.7
32	0.7079527	5.9	8.3
64	0.7079464	21	29.7
DVM			
16	0.7079473	10	14.1

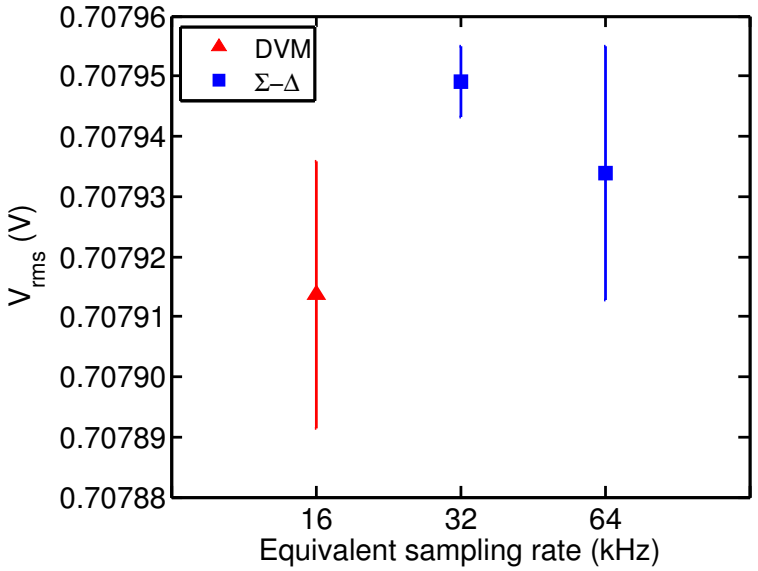


Figure 7.13: Input signal frequency 2 kHz

Table 7.13: Input signal frequency 2 kHz

Σ-Δ system			
Eq. f_s (kHz)	rms Value (V)	u_c (μV)	$\left(\frac{\mu V}{V}\right)$
32	0.7079491	5.9	8.3
64	0.7079339	21	29.7
DVM			
16	0.7079136	22	31.1

be higher than the settling time of the filters, which was determined as 24 samples (see section 5.2.5). That imposes a constraint on the ratio between the sampling rate f_s and the input signal frequency f. Hence, the ratio f_s/f must be higher than 24. Although this condition was not always fulfilled, the results are within uncertainty levels of the DVM for a coverage factor k=2.

Summarizing, in order to obtain accurate results the ratio between the sampling rate and the input signal frequency to be measured must be higher than 24, which is the measured settling time in samples of the system. With the Σ-Δ sampling system it is possible to sample signals with peak amplitudes equal to 1 V in the frequency range from

62.5 Hz to 2 kHz with a combined uncertainty of 30 μV/V at a sampling rate equal to 64 kHz. And, in the frequency range from 62.5 Hz to 1 kHz with a combined uncertainty lower than 8 μV/V at equivalent sampling rates from 4 kHz to 32 kHz, improving the performance of the DVM at 500 Hz.

7.1.3 Uncertainty Budget

The uncertainty sources which contribute to the system total uncertainty are: the system transfer function TF and the uncertainty of the correction for the anti-aliasing filters $K_{FDA}(f)$. The uncertainty budget for the particular case of an input signal with frequency 62.5 Hz sampled at an equivalent sampling rate equal to 32 kHz is listed in table 7.14.

Table 7.14: Uncertainty Budget

Input signal frequency 62.5 Hz. Equivalent Sampling Rate 32 kHz

Source	Description	Distribution	Type	c_j	u_j	$(c_j u_j)^2$ (V^2)
V_{ref}	Voltage reference	rect.	A	1	1.2 μV	
Hammerstein model	Prediction Interval	normal	A	1	5.5 μV	
Effective resolution		normal	A	1	1.7 μV	
$u(TF)$	Transfer function	normal	A	1.0000000	5.9 μV	3.2 10^{-11}
$u(K_{FDA})$	$K_{FDA}(f)$	rect.	A	0.7079620 V	7.1 10^{-10}	2.5 10^{-19}
					$\mathbf{u_c}$	**5.9 μV**

The uncertainty denoted as $u(TF)$ is the combination of the uncertainty of the voltage reference, the system resolution and the uncertainty associated when predicting the measured value using the system model (the first three rows in table 7.14). As described in section 3.2.3 the value of the voltage reference changes as the sampling rate changes, then the uncertainty contribution to the ADC readouts has been determined equal to 1.2 μV/V, assuming a rectangular probability distribution. The system effective resolution has been measured to exceed 20 bits, which corresponds to an effective resolution of 1.7 μV. The uncertainty contribution associated to the prediction of the reconstructed value is the main contribution to the total uncertainty because it includes the contribution from all the components (gain, drift, non-linearity) in the sampling system. The second uncertainty source $u(K_{FDA}(f))$ is the indeterminacy in the cut-off frequency of anti-aliasing low pass filter. The maximum contribution is bound at an input signal frequency of 2 kHz to a value equal to 0.73 μV/V (see appendix A). As the input signal frequency is lower the contribution to the total uncertainty is reduced to a level equal to $7.0 \cdot 10^{-4}$ μV/V.

7.2 Stability of the Sampling System Transfer Function

It is of particular interest to observe the short term and long term stability of the system accuracy. Thus, the system was daily calibrated during one week (short term stability) and then after two months a new calibration was performed (long term stability). The system was continuously powered.

The main contributions to the stability of the system transfer function are the thermal drift of the voltage reference IC, resistors, amplifiers and Σ-Δ ADC. All these contributions can be evaluated monitoring the evolution versus time of the Hammerstein model non-linear transfer function.

To evaluate the stability of the transfer function, the system was monitored daily during one week at the equivalent sampling rate equal to 32 kHz. At the same time, the instantaneous voltage reference value $V_{ref}(t)$ was measured to establish the correlation between the non-linear transfer function TF of the Hammerstein model and the ADC voltage reference. The transfer function TF was evaluated as if the voltage amplitude of the ADC readouts were 1 V with $f = 0\ Hz$ (DC), namely

$$V_i = TF(1\ V, 0, f_s)\,, \tag{7.3}$$

where f_s denotes the equivalent sampling rate. The results are plotted in figure 7.14 and show that the values of TF during the measuring period are within the uncertainty

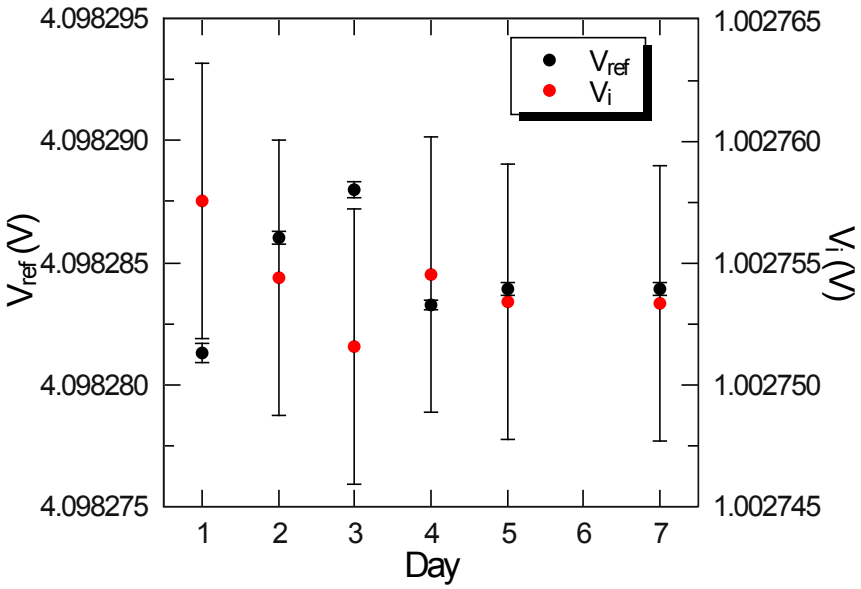


Figure 7.14: Non-linear transfer function $TF(1\ V, 0, 32\ kHz)$ short term stability. Equivalent sampling rate 32 kHz. The type-A uncertainty bars correspond to a coverage factor k=1

limits. Besides, it is clear to see the inverse dependence of TF with the voltage reference

value as stated by equation (3.14).

An analysis can be performed to find the correlation between the ADC output binary code and the voltage reference value $V_{ref}(t)$.

The block diagram shown in figure 7.15 indicates the input signal $V_i(t)$ path through the complete system and how it is affected by the gains of the different system's stages.

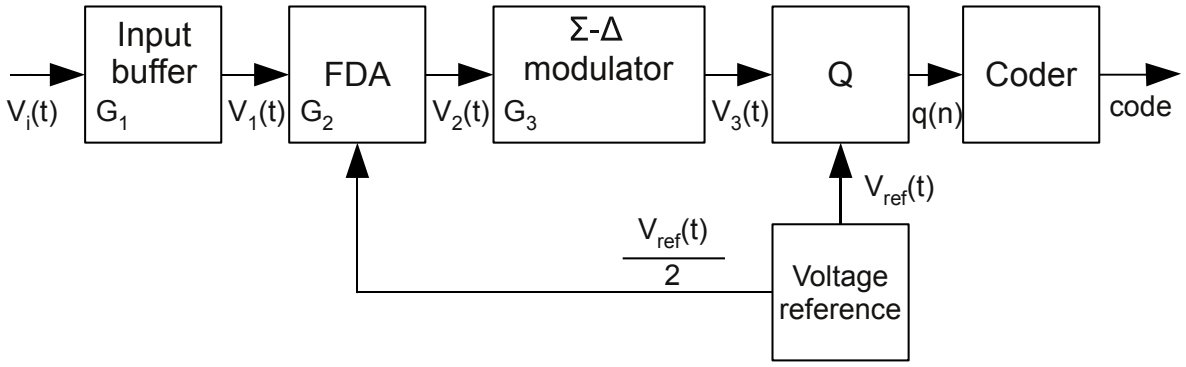


Figure 7.15: Simplified block diagram of the sampling system showing the input signal $V_i(t)$ path through the different system's stages

The correlation can be described by the following analysis. The output of a mid-tread quantizer, as stated by equations (3.13) and (3.14), is inversely proportional to its voltage reference. The input $q(n)$ of the coder are the quantized values of the output of the Σ-Δ modulator $V_3(t)$

$$q(n) = Q[V_3(t)] = \left\lfloor V_3(t)\frac{2^N}{FSR} + \frac{1}{2} \right\rfloor, \tag{7.4}$$

where N is the ADC resolution in bits and FSR is the ADC full-scale range. For the particular device used in this thesis FSR is equal to $0.8\,V_{ref}(t)$ [27], hence

$$q(n) = \left\lfloor V_3(t)\frac{2^N}{0.8\,V_{ref}(t)} + \frac{1}{2} \right\rfloor, \tag{7.5}$$

$V_{ref}(t)$ is the value of the system voltage reference at time t.

The outputs of the input buffer $V_1(t)$, the FDA $V_2(t)$ and the Σ-Δ modulator $V_3(t)$ are (supposing a linear transfer function for the sake of simplicity)

$$V_1(t) = G_1\,V_i(t) + V_{off_1} \tag{7.6}$$

$$V_2(t) = G_2\,V_1(t) + V_{off_2} + \frac{V_{ref}(t)}{2} \tag{7.7}$$

$$V_3(t) = G_3\,V_2(t) + V_{off_3} \tag{7.8}$$

Replacing equations (7.6), (7.7) and (7.8) in equation (7.5)

$$\begin{aligned} q(n) &= \left\lfloor (G_3 V_2(t) + V_{off_3}) \frac{2^N}{0.8 V_{ref}(t)} + \frac{1}{2} \right\rfloor \\ &= \left\lfloor \left(G_3 \left(G_2 V_1(t) + V_{off_2} + \frac{V_{ref}(t)}{2} \right) + V_{off_3} \right) \frac{2^N}{0.8\, V_{ref}(t)} + \frac{1}{2} \right\rfloor \\ &= \left\lfloor \left(G_3 \left(G_2 \left(G_1 V_i(t) + V_{off_1} \right) + V_{off_2} + \frac{V_{ref}(t)}{2} \right) + V_{off_3} \right) \frac{2^N}{0.8\, V_{ref}(t)} + \frac{1}{2} \right\rfloor , \end{aligned} \tag{7.9}$$

rearranging equation (7.9) it becomes

$$\begin{aligned} q(n) &= \left\lfloor \left(G_3\, G_2\, G_1\, V_i(t) + G_3\, G_2\, V_{off_1} + G_3\, V_{off_2} + V_{off_3} + G_3 \frac{V_{ref}(t)}{2} \right) \frac{2^N}{0.8\, V_{ref}(t)} + \frac{1}{2} \right\rfloor \\ &= \left\lfloor \left(G_T\, V_i(t) + V_{off} + G_3 \frac{V_{ref}(t)}{2} \right) \frac{2^N}{0.8\, V_{ref}(t)} + \frac{1}{2} \right\rfloor , \end{aligned} \tag{7.10}$$

where

$$G_T = G_3\, G_2\, G_1 \quad \text{and} \quad V_{off} = G_3\, G_2\, V_{off_1} + G_3\, V_{off_2} + V_{off_3}\,.$$

The ADC employs a bipolar codification [21] to obtain the output digital *code*, as a consequence the input to the coder $q(n)$ (see figure 7.15) is scaled to the middle scale factor equal to $2^{(N-1)}$, thus

$$\begin{aligned} \text{code} &= q(n) - 2^{(N-1)} \\ &= \left\lfloor \left(G_T\, V_i(t) + V_{off} + G_3 \frac{V_{ref}(t)}{2} \right) \frac{2^N}{0.8\, V_{ref}(t)} + \frac{1}{2} \right\rfloor - 2^{(N-1)} \\ &= \left\lfloor \left(G_T\, V_i(t) + V_{off} + G_3 \frac{V_{ref}(t)}{2} \right) \frac{2^{(N-1)}}{0.8 \dfrac{V_{ref}(t)}{2}} + \frac{1}{2} \right\rfloor - 2^{(N-1)}\,. \end{aligned} \tag{7.11}$$

The output digital code is then converted to voltage using the following scaling equation

$$V_o(n) = \text{code} \cdot \frac{FS_{nom}}{2^{(N-1)}} = \text{code} \cdot \frac{V_{ref}}{2^{(N-1)}} \tag{7.12}$$

Replacing equation (7.11) in equation (7.12) results

$$
\begin{aligned}
V_o(n) &= \left\lfloor \left(\left(G_T\, V_i(t) + V_{off} + G_3\, \frac{V_{ref}(t)}{2} \right) \frac{2^{(N-1)}}{0.8\, \dfrac{V_{ref}(t)}{2}} + \frac{1}{2} \right\rfloor - 2^{(N-1)} \right) \cdot \frac{V_{ref}}{2^{(N-1)}} \\
&= \left\lfloor \left(G_T\, V_i(t) + V_{off} + G_3\, \frac{V_{ref}(t)}{2} \right) \frac{2^N}{0.8\, V_{ref}(t)} + \frac{1}{2} \right\rfloor \frac{V_{ref}}{2^{(N-1)}} - V_{ref} \\
&= \left\lfloor \left(\frac{G_T\, V_i(t)}{0.8\, V_{ref}(t)} + \frac{V_{off}}{0.8\, V_{ref}(t)} + \frac{G_3}{2} \right) 2^N + \frac{1}{2} \right\rfloor \frac{V_{ref}}{2^{(N-1)}} - V_{ref} \qquad (7.13)
\end{aligned}
$$

Equation (7.13) shows that the ADC output voltage $V_o(n)$ is inversely proportional to the instantaneous value of the voltage reference $V_{ref}(t)$. This dependence can be observed in figure 7.14.

As a final evaluation, the system model parameters have been obtained and the transfer function has been evaluated using equation (7.3) after a period of two months. Figure 7.16 compares measurement results two months apart and shows that the system transfer function is within the uncertainty level for k=1.

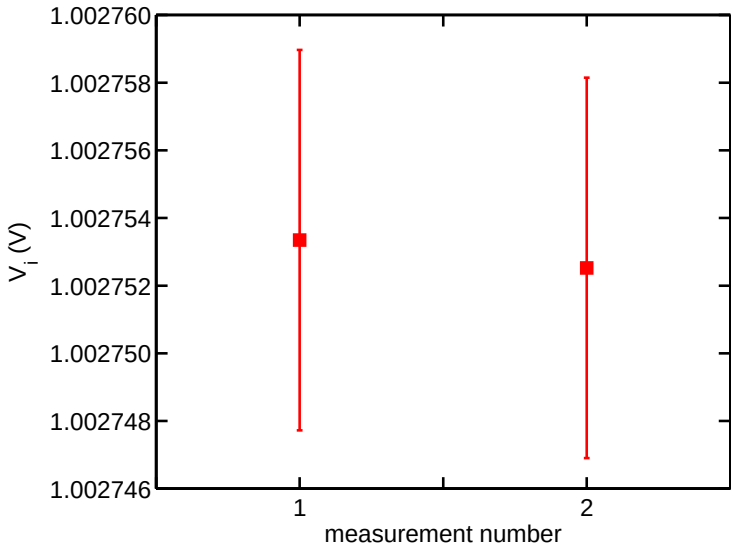


Figure 7.16: System model transfer function comparison. Interval between measurements 2 months

These results show that the system is stable, within the uncertainty limits, during a period of time more than two months. This is of particular interest when performing long term measurements. Further measurements are required to set the exact recalibration interval to stay within this uncertainty. It is however clear that, for a continuously powered system, recalibration would be required less frequently than every two months.

Chapter 8

Conclusion and Outlook

A high resolution sampling system based on a Σ-Δ ADC has been developed and characterized. The experimental results confirmed that the estimated combined uncertainty is 8 μV/V (k=1) at the equivalent sampling rate of 32 kHz (BW=16 kHz), when measuring a sinusoidal signal with 1 V nominal peak amplitude in the frequency range from 62.5 Hz to 1.3 kHz. Compared to the performance of the *de facto* standard for sampling systems, these uncertainties show that the designed sampling system improves the uncertainty achievable with *de facto* standard which reaches 8 μV/V at 500 Hz and can be used for ac metrology.

A model has been established for the system in order to reconstruct the signal at the input from the readings of the ADC. The parameters for this model were determined using Josephson waveforms. The model was then validated by comparing measurements of the rms value of a sinusoidal signal with the established measurement unit *de facto* standard in metrology. The validation results have shown that the Hammerstein model compensates the Σ-Δ sampling system readouts for non-linearity and frequency response of the decimation filters. Using a fourth order polynomial the non-linearities have been reduced from 150 μV/V to 40 μV/V (k=2) at the worst case, which corresponds to the equivalent sampling rate equal to 64 kHz. At the equivalent sampling rate of 32 kHz the non-linearities have been compensated to a limit below 10 μV/V (k=2), and at lower sampling rates the non-linearities are below 6 μV/V (k=2).

The effective resolution over an input range of 1 V has been measured to exceed 20 bits, at the equivalent sampling rate of 32 kHz. In comparison with the *de facto* standard system, which reaches this resolution at a sampling rate lower than 10 kHz. The settling time for the complete system has been determined as 24 samples, this parameter limits the ratio between the sampling rates and the input signal frequency to be higher than 24. Furthermore, it is an important parameter when measuring power quality parameters or multiplexed signals.

In addition, the stability in time of the system parameters required in the model was also established, in the short term by repeating the Josephson calibration daily over one week, and for long term after two months. The drift of the transfer function during the one week interval and after two months is considerably lower than the uncertainty limit of 6 μV/V which is required on the model parameters. Further measurements are required to set the exact recalibration interval to stay within this uncertainty. It is however clear that recalibration would be required less frequently than every two months, for a continuously powered system.

8.1 Outlook

The studies carried out in this thesis open up new improvements for the system designed. The input range may be increased to ± 4 V by means of either adding a resistive voltage divider at the system input or by changing the gain of the input stage.

For power measurements or voltage ratio measurements a fast and low impedance switch may be used to measure the different quantities using the same ADC (including the signal conditioning circuitry), or a second ADC can be added to sample the second quantity. The second solution implies to build a second board with similar performance and to synchronize both boards.

Sigma-Delta ADCs are complex devices, thus a good knowledge of their internal structure is required in order to model the system for post-compensation. For metrology applications, or for all high accuracy and performance applications, it would be useful to work closely with the designers of the Σ-Δ ADC.

Appendix A

A.1 Anti-aliasing Filters Uncertainty Estimation

The fully differential amplifier (FDA) was configured as a double pole anti-aliasing filter, in consequence the input signal is attenuated by the gain of this filters and it must be corrected. The compensation to the ADC readouts due to the FDA anti-aliasing filters is given by the following equation

$$K_{FDA}(f) = \sqrt{1 + \left(\frac{f}{f_{p1}}\right)^2} \cdot \sqrt{1 + \left(\frac{f}{f_{p2}}\right)^2}, \tag{A.1}$$

where $f_{p1} = 1/(2\pi R_f C_f)$ is the frequency of the first pole and $f_{p2} = 1/(2\pi R_s 2C_s)$ is the frequency of the second pole.

The uncertainty contribution to the final value may be calculated as the squared root of the variance $u^2(K_{FDA})$

$$u^2(K_{FDA}) = \left(\frac{\partial K_{FDA}(f)}{\partial f_{p1}}\right)^2 u^2(f_{p1}) + \left(\frac{\partial K_{FDA}(f)}{\partial f_{p2}}\right)^2 u^2(f_{p2}) \tag{A.2}$$

where

$$\frac{\partial K_{FDA}(f)}{\partial f_{p1}} = -\frac{f^2\left(1 + \frac{f^2}{f_{p2}^2}\right)^{0.5}}{\left(1 + \frac{f^2}{f_{p1}^2}\right)^{0.5} f_{p1}^3}$$

and

$$\frac{\partial K_{FDA}(f)}{\partial f_{p2}} = -\frac{f^2\left(1 + \frac{f^2}{f_{p1}^2}\right)^{0.5}}{\left(1 + \frac{f^2}{f_{p2}^2}\right)^{0.5} f_{p2}^3},$$

are the sensitive coefficients.

The uncertainty on the cut-off frequencies f_{p1} and f_{p2} are caused by mismatches in the passive electronic components R_f, C_f and R_s, C_s, respectively. Assuming the tolerance

of these components as uncertainty ($u(R)$=100 $\mu\Omega/\Omega$ and $u(C)$=5%), with a rectangular distribution [56], the uncertainty of f_{p1} can be estimated as

$$\begin{aligned} u^2(f_{p1}) &= \left(\frac{\partial f_{p1}}{\partial R_f}\right)^2 u^2(R_f) + \left(\frac{\partial f_{p1}}{\partial C_f}\right)^2 u^2(C_f) \\ &= \left(-\frac{1}{2\pi C_f R_f^2}\right)^2 u^2(R_f) + \left(-\frac{1}{2\pi R_f C_f^2}\right)^2 u^2(C_f) \end{aligned} \tag{A.3}$$

Similarly, the uncertainty of f_{p2} is

$$\begin{aligned} u^2(f_{p2}) &= \left(\frac{\partial f_{p2}}{\partial R_s}\right)^2 u^2(R_s) + \left(\frac{\partial f_{p2}}{\partial C_s}\right)^2 u^2(C_s) \\ &= \left(-\frac{1}{4\pi C_s R_s^2}\right)^2 u^2(R_s) + \left(-\frac{1}{4\pi R_s C_s^2}\right)^2 u^2(C_s) \end{aligned} \tag{A.4}$$

The total contributions to the uncertainty are listed in table A.1, for certain input signal frequencies of interest.

Table A.1: Uncertainty contribution of the FDA anti-aliasing filters

Input signal frequency (Hz)	uncertainty (10^{-6})
62.5	7.12 10^{-4}
125	2.85 10^{-3}
250	1.14 10^{-2}
500	4.56 10^{-2}
1000	1.82 10^{-1}
2000	7.29 10^{-1}

As can be deduced from these results, the uncertainty contributions due to the anti-aliasing filter to the total uncertainty are bound to $0.7 \cdot 10^{-6}$ when the input signal frequency is 2 kHz, and decrease to $0.7 \cdot 10^{-9}$.

A.2 Zero-order Hold Uncertainty Estimation

The sampling process involves to observe the input signal during a finite time at equidistant time intervals defined by the sampling time. This process can be described as the convolution of the input signal with a train of pulses of finite width. This process is referred as sampling with a zero-order hold (ZOH). As a consequence, the input signal

is affected by the transfer function of the zero-order hold and needs to be compensated. The compensation for the ZOH is given by the following expression

$$K_{ZOH}(f, f_s) = \frac{(\pi\, f/(2f_s))}{\sin\left(\pi\, f/(2f_s)\right)}\,. \tag{A.5}$$

The uncertainty $u(K_{ZOH})$ is the indeterminate value of the sampling rate f_s and can be calculated

$$u(K_{ZOH}) = \left|\frac{\partial K_{ZOH}(f, f_s)}{\partial f_s}\right| u(f_s)\,, \tag{A.6}$$

where

$$\frac{\partial K_{ZOH}}{\partial f_s} = \frac{\pi^2\, f^2 \cos\left(\frac{\pi\, f}{2f_s}\right)}{4\sin^2\left(\frac{\pi\, f}{2f_s}\right) {f_s}^3} - \frac{\pi\, f}{2\sin\left(\frac{\pi\, f}{2f_s}\right)\ {f_s}^2}\,.$$

The main contribution to $u(f_s)$ comes from the accuracy of the reference clock (internal or external) which supplies the system the sampling clock; with an internal clock with an accuracy of 100 μHz/Hz, supposing a rectangular distribution. The uncertainty contribution to the final value is listed in table A.2, for certain input signal frequencies of interest.

Table A.2: Uncertainty due to the ZOH compensation

	input signal frequency (Hz)					
f_s	62.5	125	250	500	1000	2000
(kHz)	uncertainty (10^{-6})					
16384	$0.7\ 10^{-9}$	$3\ 10^{-9}$	$1\ 10^{-8}$	$4\ 10^{-8}$	$2\ 10^{-7}$	$7\ 10^{-7}$
8192	$3\ 10^{-9}$	$1\ 10^{-8}$	$4\ 10^{-8}$	$2\ 10^{-7}$	$7\ 10^{-7}$	$3\ 10^{-6}$
4096	$1\ 10^{-8}$	$4\ 10^{-8}$	$2\ 10^{-7}$	$7\ 10^{-7}$	$3\ 10^{-6}$	$1\ 10^{-5}$
2048	$4\ 10^{-8}$	$2\ 10^{-7}$	$7\ 10^{-7}$	$3\ 10^{-6}$	$1\ 10^{-5}$	$5\ 10^{-5}$
1024	$2\ 10^{-7}$	$7\ 10^{-7}$	$3\ 10^{-6}$	$1\ 10^{-5}$	$5\ 10^{-5}$	$2\ 10^{-4}$

Because the ratio between the sampling rate and the input signal frequency is high and the sensitivity coefficients are inversely proportional to the sampling rate, which is higher than 1 MHz, as a consequence, the uncertainties are below of some parts in 10^8, as can be seen in table A.2. Thus the contribution of the uncertainty of the ZOH compensation to the final value can be considered negligible.

A.3 Sinc Correction Uncertainty Estimation

The rms value of the sampled signal must be corrected from the finite number of samples. This correction is given by

$$K_{sinc}(f, f_s) = K_{sinc_1}(f, f_s) \cdot K_{sinc_2}(f, f_s) \cdot K_{sinc_3}(f, f_s)\,, \tag{A.7}$$

with

$$K_{sinc_i}(f, f_s) = \frac{\pi f f_s^{-1} M_i}{\sin(\pi f f_s^{-1} M_i)}$$

where f is the input signal fundamental frequency, f_s is the Σ-Δ modulator sampling rate and M_i (with $i = 1, 2, 3$) is the corresponding decimation factor of each stage, i.e. $M_1 = 4$, $M_2 = 32$ and $M_3 = 2$.

Assuming that K_{sinc_i} are uncorrelated and have uncertainty $u(K_{sinc_i})$, applying the propagation law, the variance of $K_{sinc}(f, f_s)$ can be expressed as

$$u^2(K_{sinc})(f, f_s) = u^2(K_{sinc_1}) + u^2(K_{sinc_2}) + u^2(K_{sinc_3})\,. \tag{A.8}$$

where

$$\begin{aligned}
u(K_{sinc_1}) &= \left(\frac{16\,\pi^2 f^2 \cos(4\,\pi f/f_s)}{f_s^3 \sin(4\,\pi f/f_s)} - \frac{4\,\pi f}{f_s^2 \sin(4\,\pi f/f_s)}\right) \cdot u(f_s) \\
u(K_{sinc_2}) &= \left(\frac{1024\,\pi^2 f^2 \cos(32\,\pi f/f_s)}{f_s^3 \sin(32\,\pi f/f_s)} - \frac{32\,\pi f}{f_s^2 \sin(32\,\pi f/f_s)}\right) \cdot u(f_s) \\
u(K_{sinc_2}) &= \left(\frac{4\,\pi^2 f^2 \cos(2\,\pi f/f_s)}{f_s^3 \sin(2\,\pi f/f_s)} - \frac{2\,\pi f}{f_s^2 \sin(2\,\pi f/f_s)}\right) \cdot u(f_s)
\end{aligned}$$

The contribution to $u(K_{sinc_i})$, as in the case of the ZOH compensation, is due to the accuracy of the sampling frequency. With a clock uncertainty of 100 μHz/Hz, supposing a rectangular distribution. The uncertainty contribution to the final value is listed in table A.3, for certain input signal frequencies of interest.

Table A.3: Uncertainty due to the K_{sinc} compensation

	input signal frequency (Hz)					
f_s	62.5	125	250	500	1000	2000
(kHz)	uncertainty (10^{-6})					
16384	$3\ 10^{-6}$	$1\ 10^{-5}$	$5\ 10^{-5}$	$2\ 10^{-4}$	$7\ 10^{-4}$	$3\ 10^{-3}$
8192	$1\ 10^{-5}$	$5\ 10^{-5}$	$2\ 10^{-4}$	$7\ 10^{-4}$	$3\ 10^{-3}$	$1\ 10^{-2}$
4096	$5\ 10^{-5}$	$2\ 10^{-4}$	$7\ 10^{-4}$	$3\ 10^{-3}$	$1\ 10^{-2}$	$5\ 10^{-2}$
2048	$2\ 10^{-4}$	$7\ 10^{-4}$	$3\ 10^{-3}$	$1\ 10^{-2}$	$5\ 10^{-2}$	$2\ 10^{-1}$
1024	$7\ 10^{-4}$	$3\ 10^{-3}$	$1\ 10^{-2}$	$5\ 10^{-2}$	$2\ 10^{-1}$	$7\ 10^{-1}$

As it has been stated in last section, the ratio between the sampling rate and the input signal frequency is high, and the sensitivity coefficients are inversely proportional to the sampling rate squared, which is higher than 1 MHz. As a consequence, the uncertainties are below of some parts in 10^8, as can be seen in table A.3, thus the contribution of the uncertainty of the sinc correction to the final value can be considered negligible.

Appendix B

In this appendix the schematic circuits of the Σ-Δ ADC, the voltage reference and the fully differential amplifier are shown.

B.1 Sigma-Delta ADC Schematic Circuit

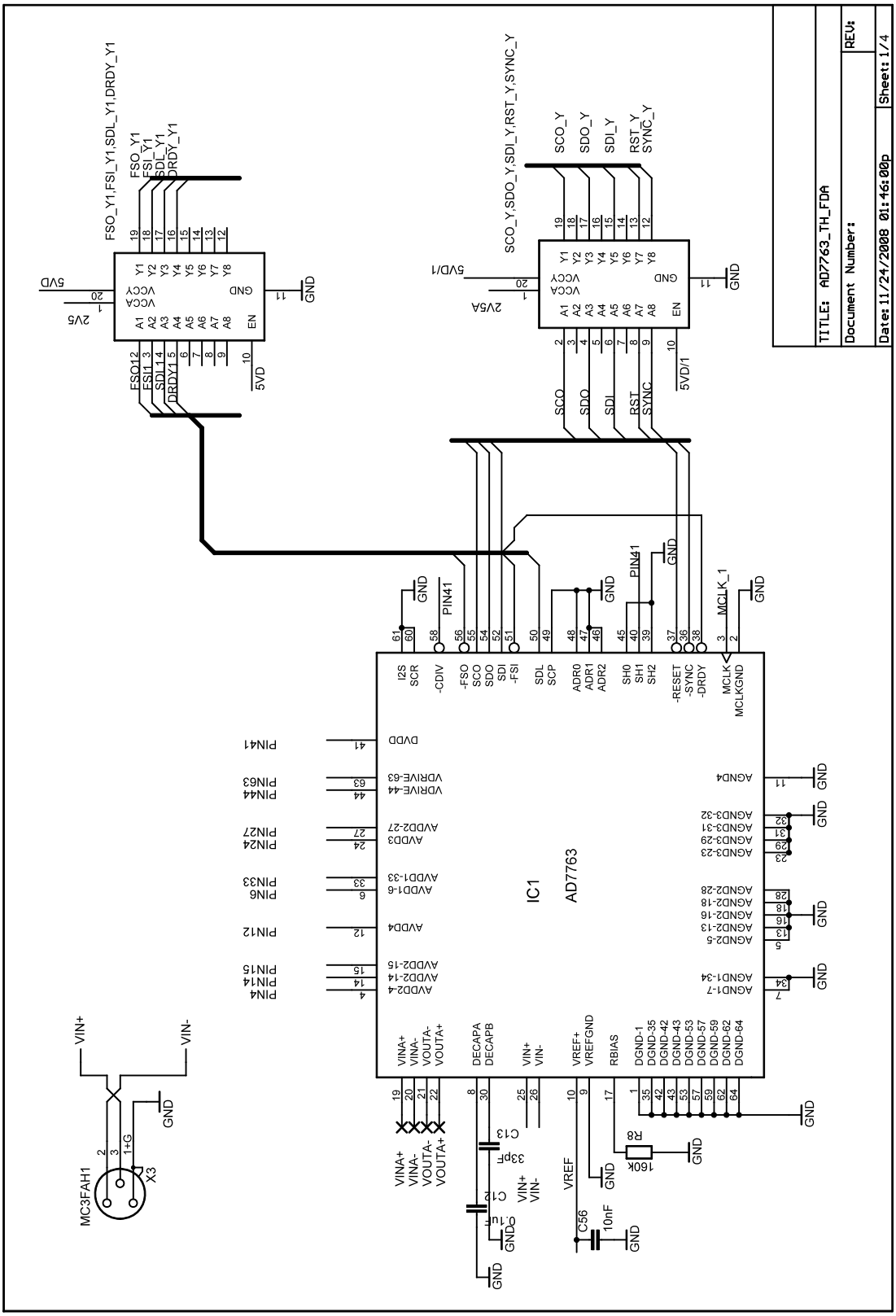


Figure B.1: Σ-Δ ADC schematic circuit sheet 1 of 4

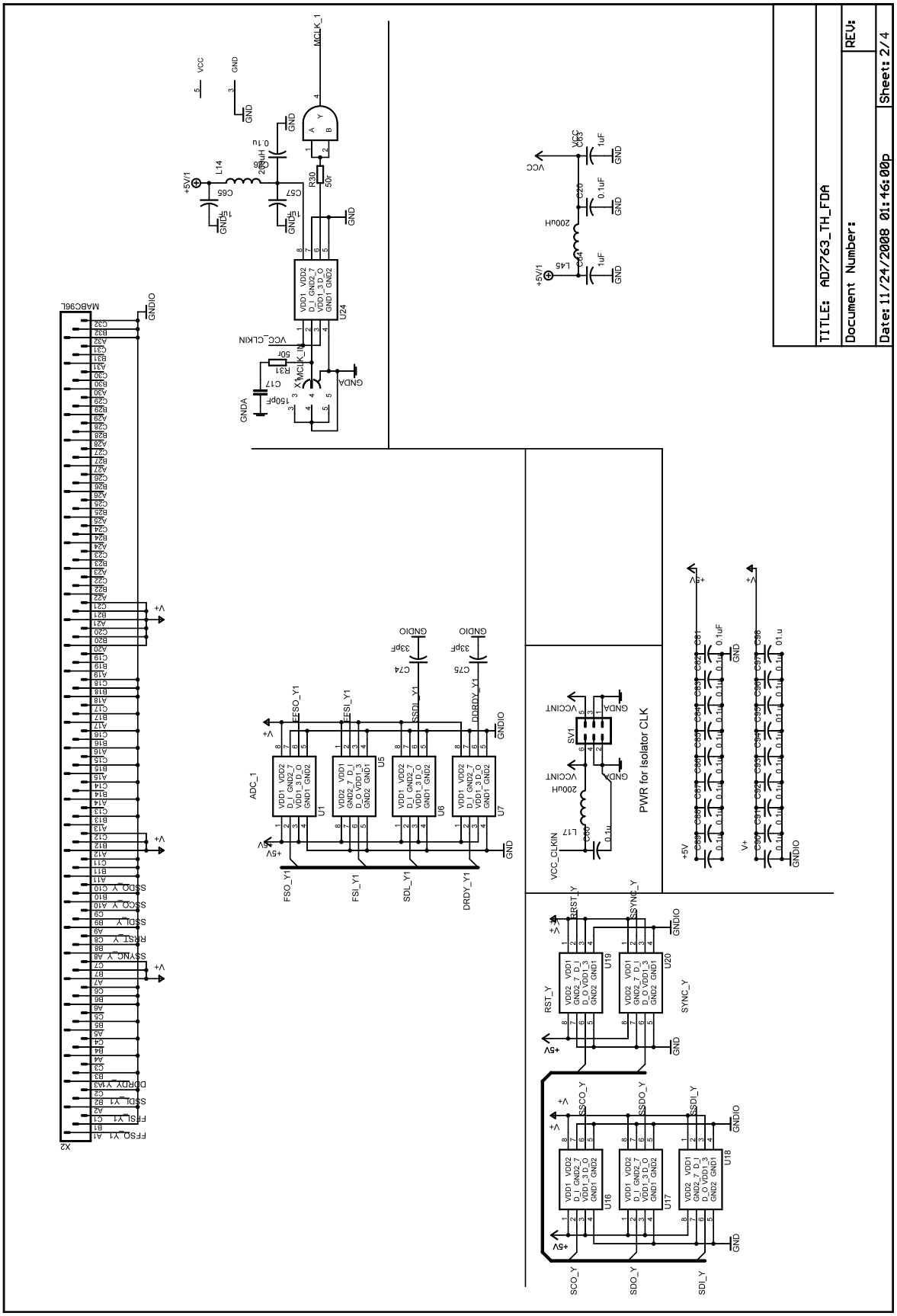


Figure B.2: Σ-Δ ADC schematic circuit sheet 2 of 4

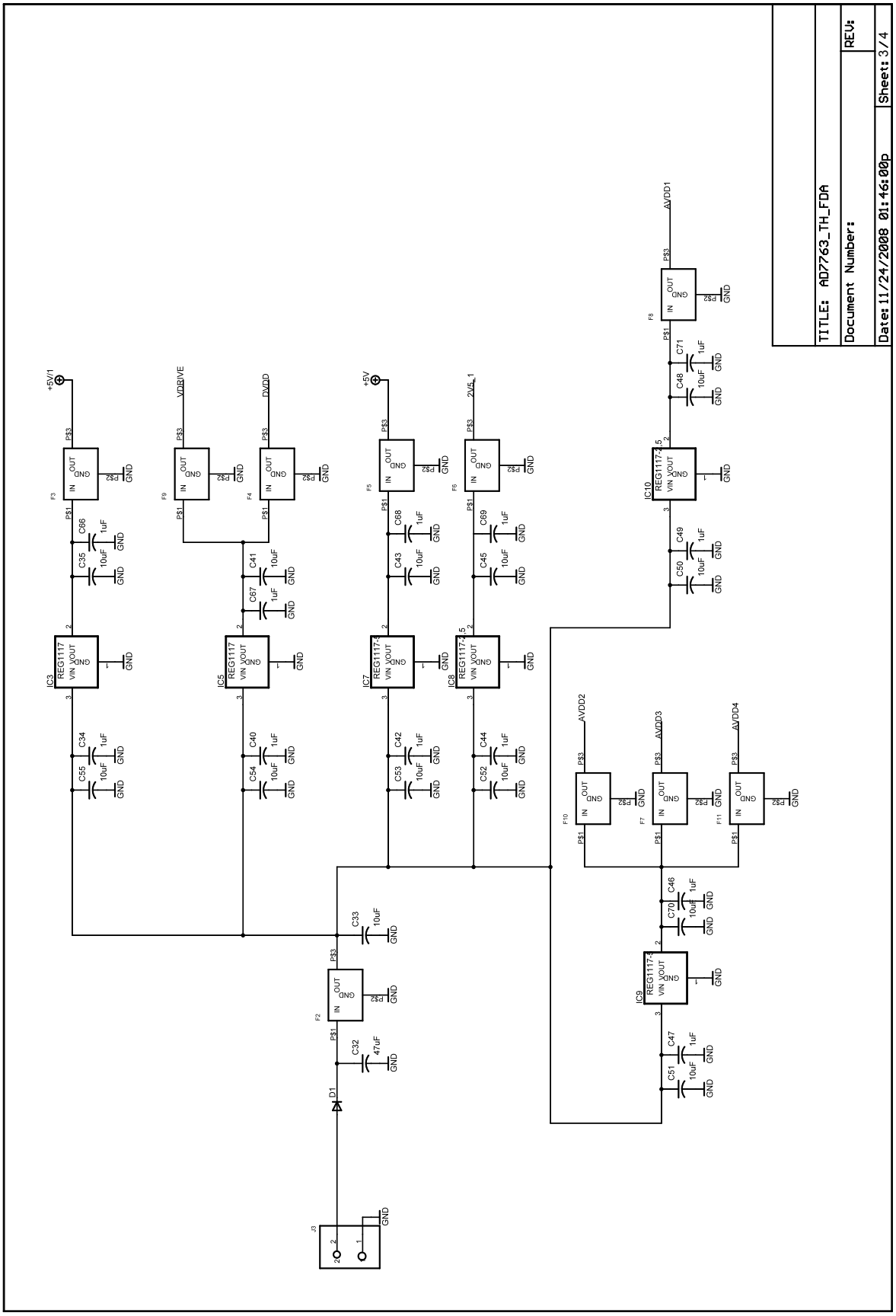


Figure B.3: Σ-Δ ADC schematic circuit sheet 3 of 4

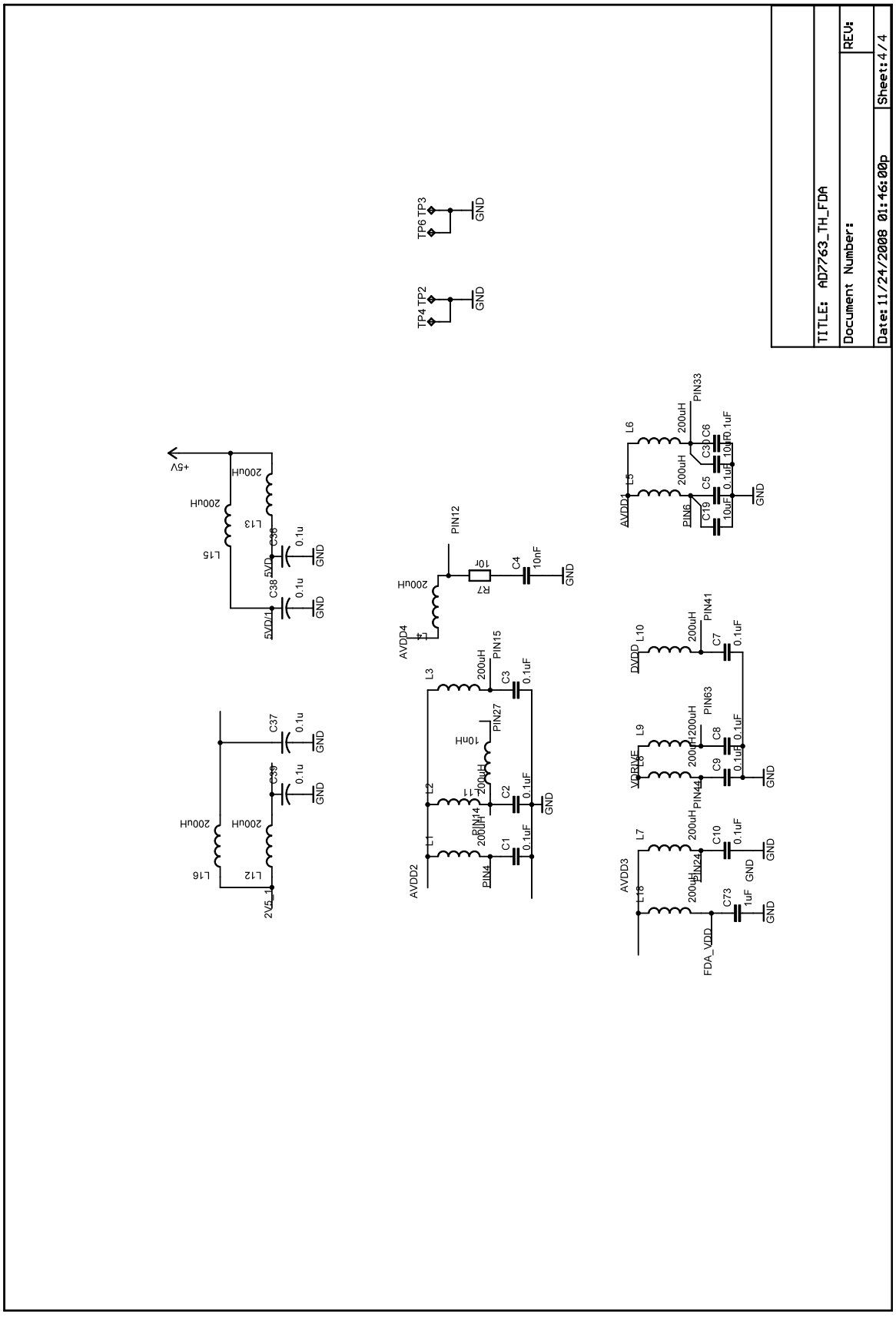


Figure B.4: Σ-Δ ADC schematic circuit sheet 4 of 4

B.2 Voltage Reference Schematic Circuit

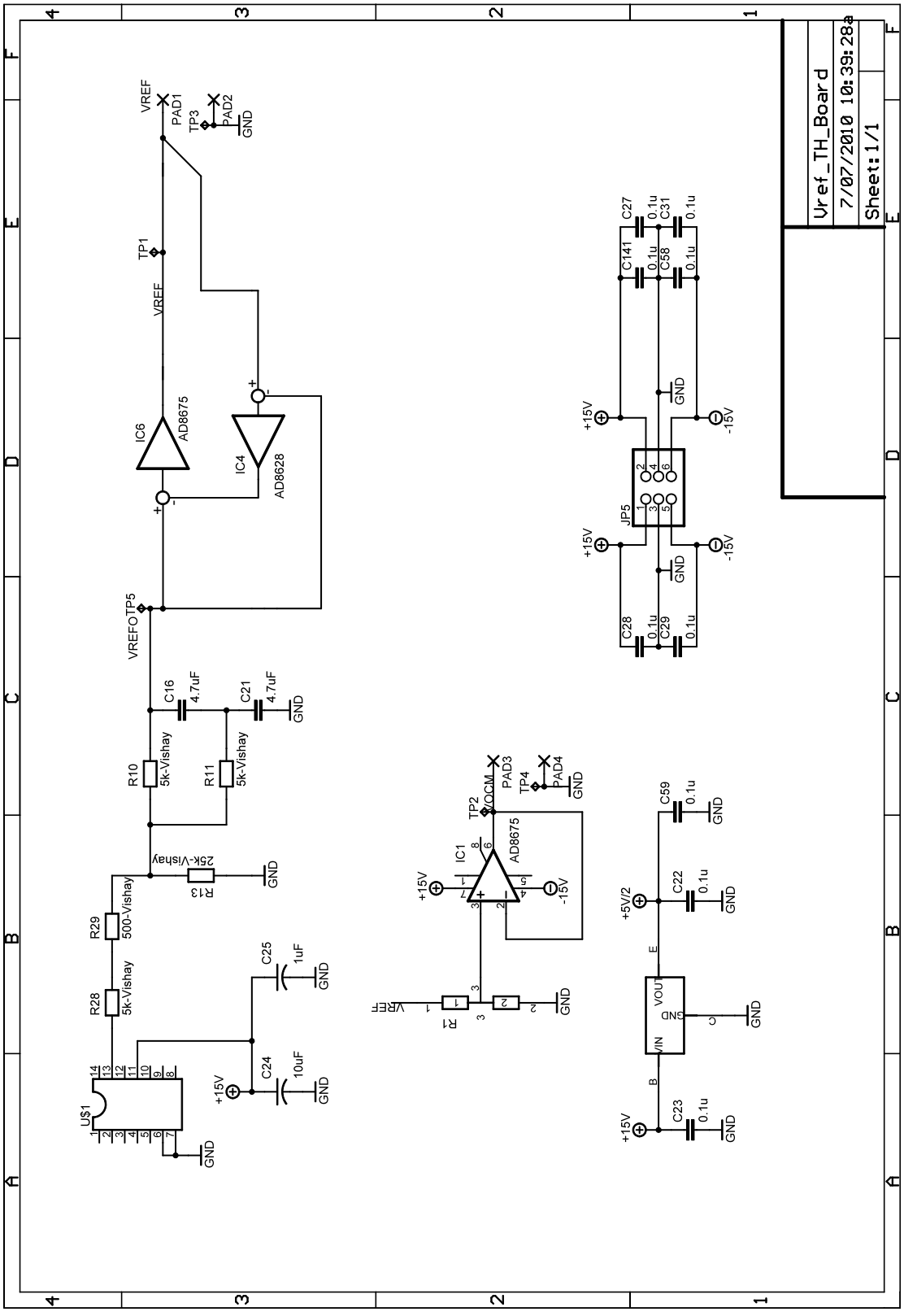


Figure B.5: Voltage reference schematic circuit

B.3 Fully Differential Amplifier Schematic Circuit

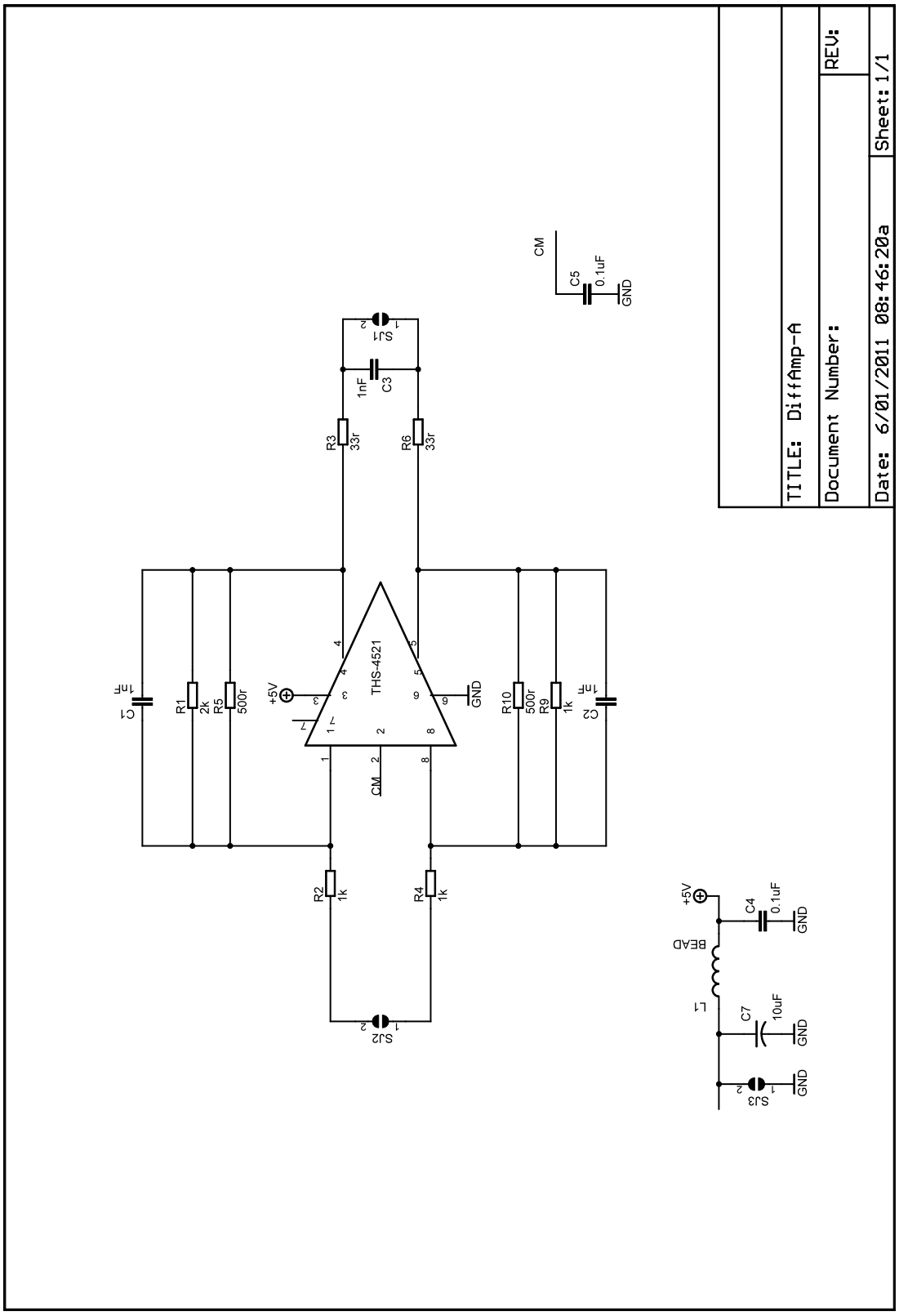


Figure B.6: Fully differential amplifier schematic circuit

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Declaration

This thesis is a presentation of my original research work. Wherever contributions of others are involved, every effort is made to indicate this clearly, with due reference to the literature, and acknowledgement of collaborative research and discussions.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;

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5. I have acknowledged all main sources of help.